

Fig. 1A

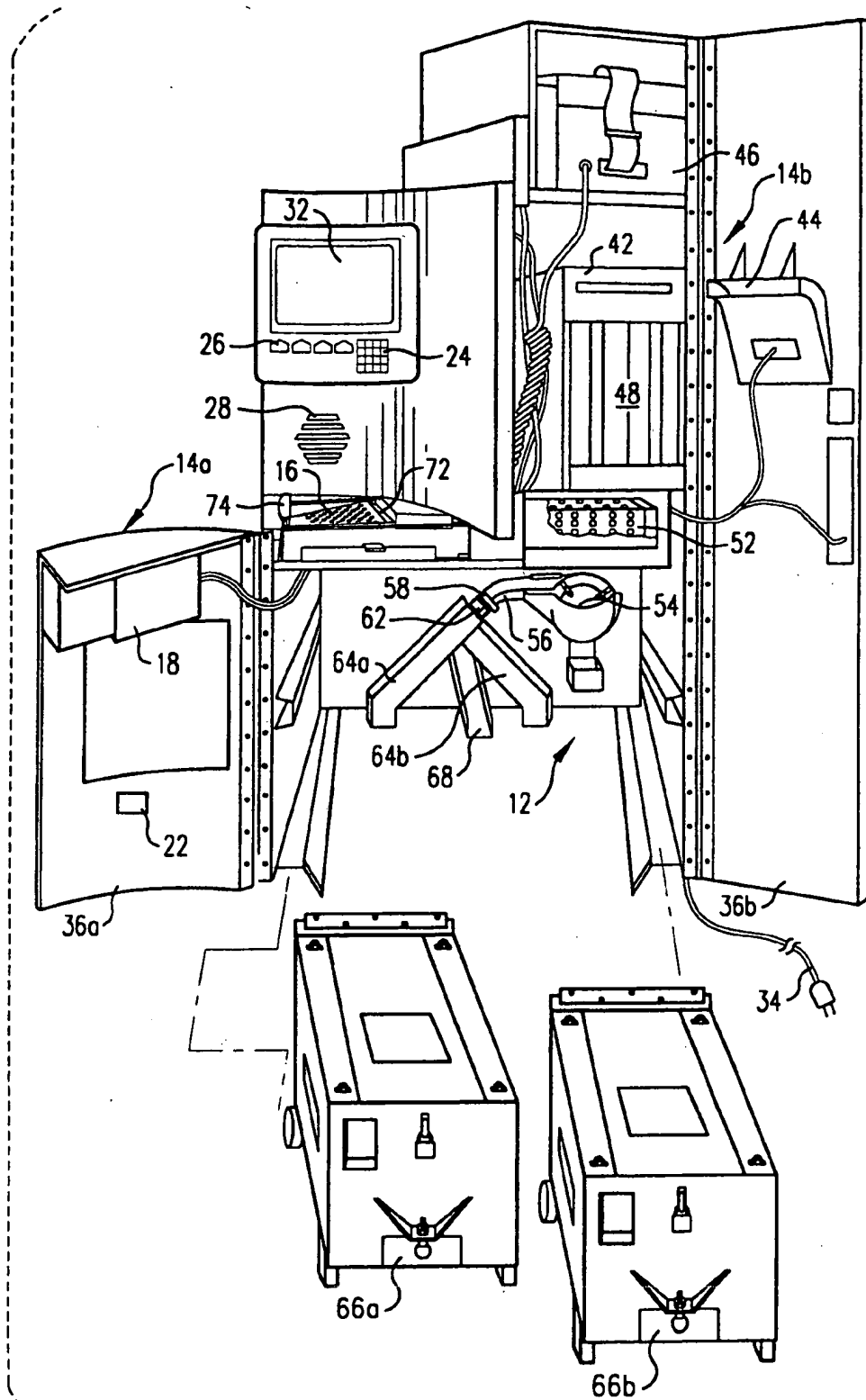


Fig. 1B

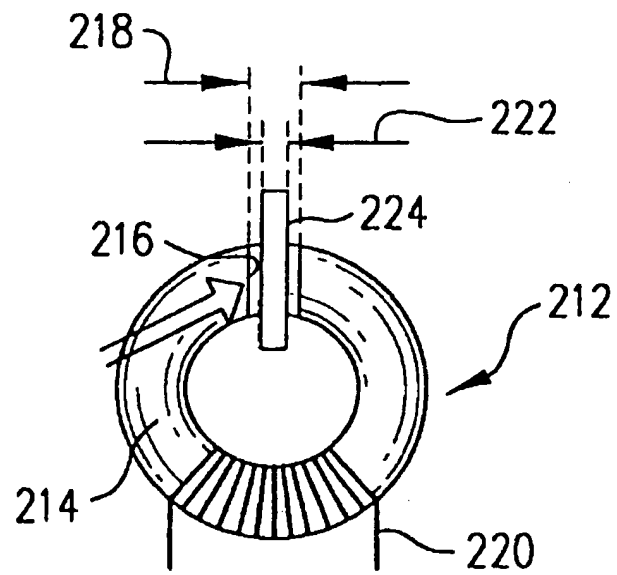


Fig. 2A

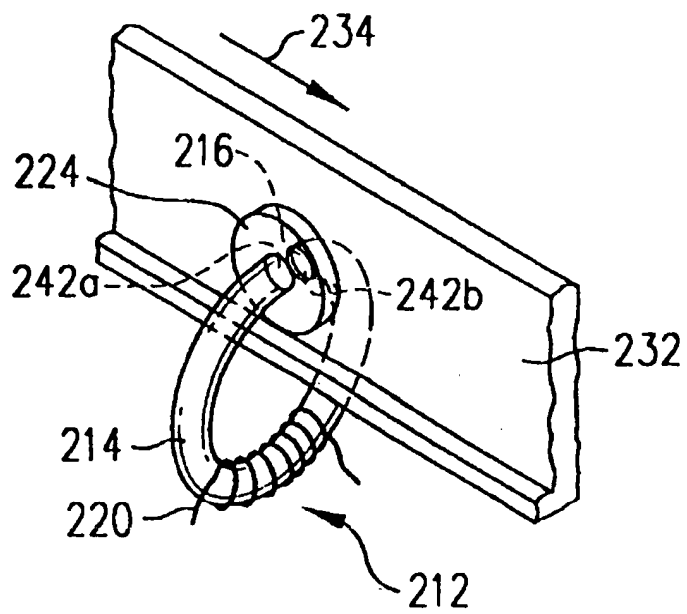


Fig. 2B

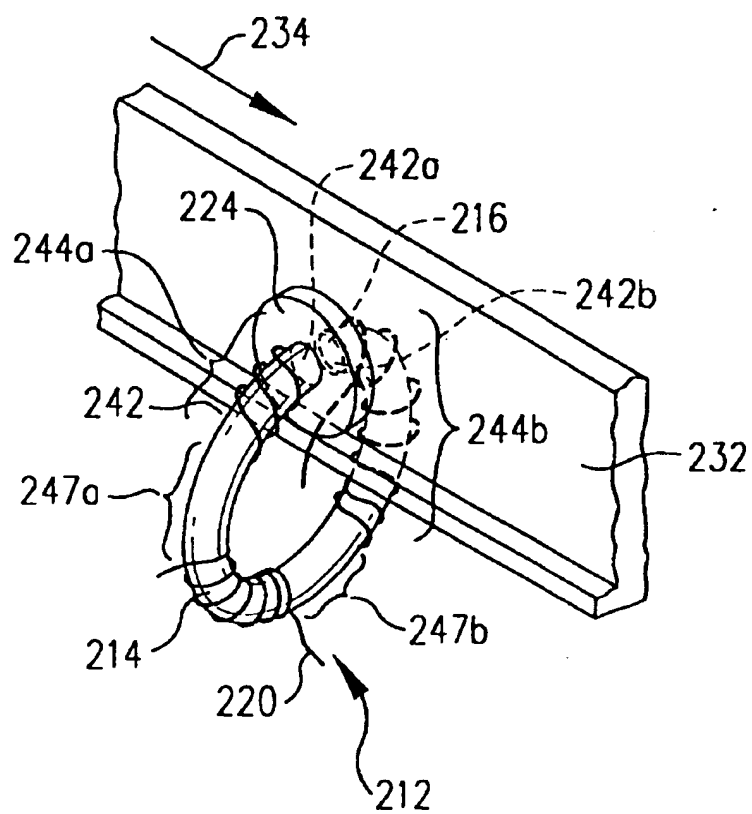


Fig. 2C

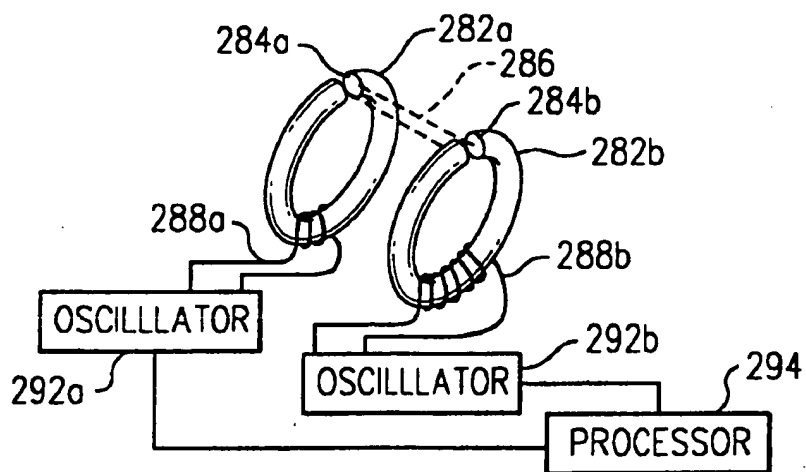


Fig. 2D

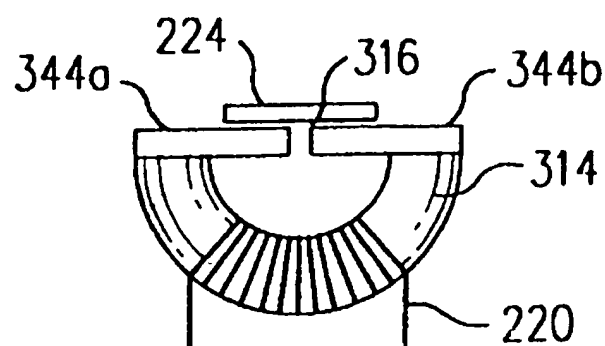


Fig. 3

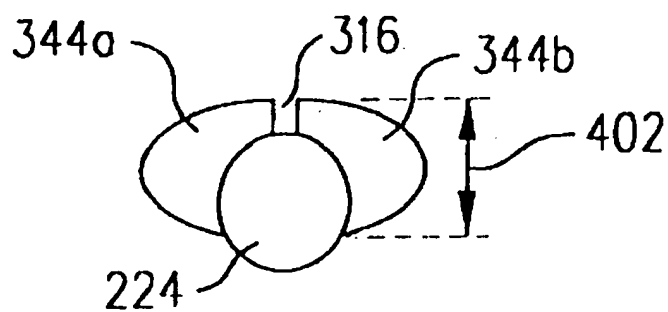


Fig. 4

FIG. 31A	FIG. 31B	FIG. 31C	FIG. 31D	FIG. 31E
	FIG. 31F	FIG. 31G	FIG. 31H	FIG. 31 I

Fig. 31

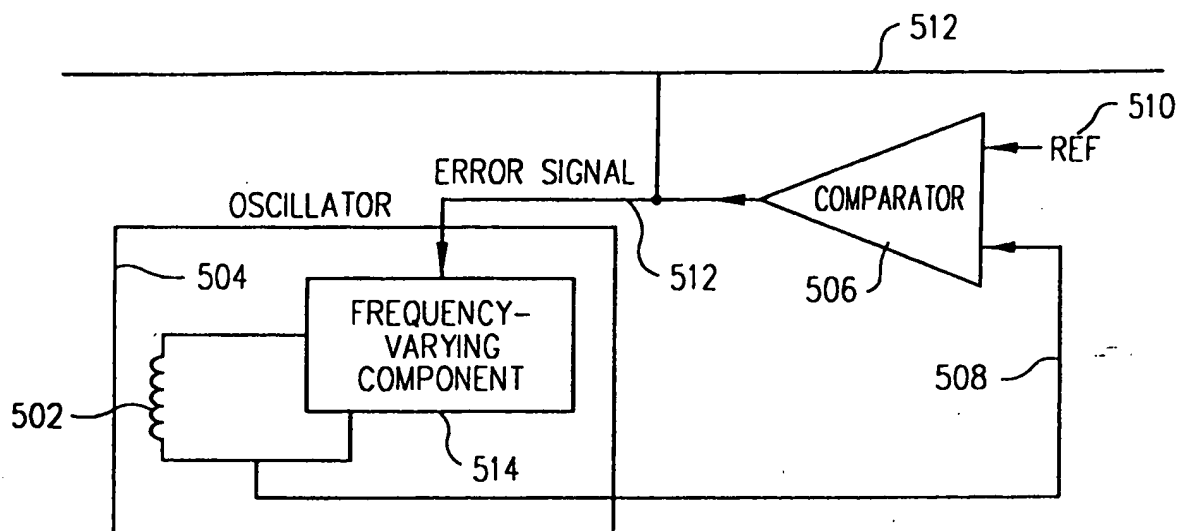


Fig. 5

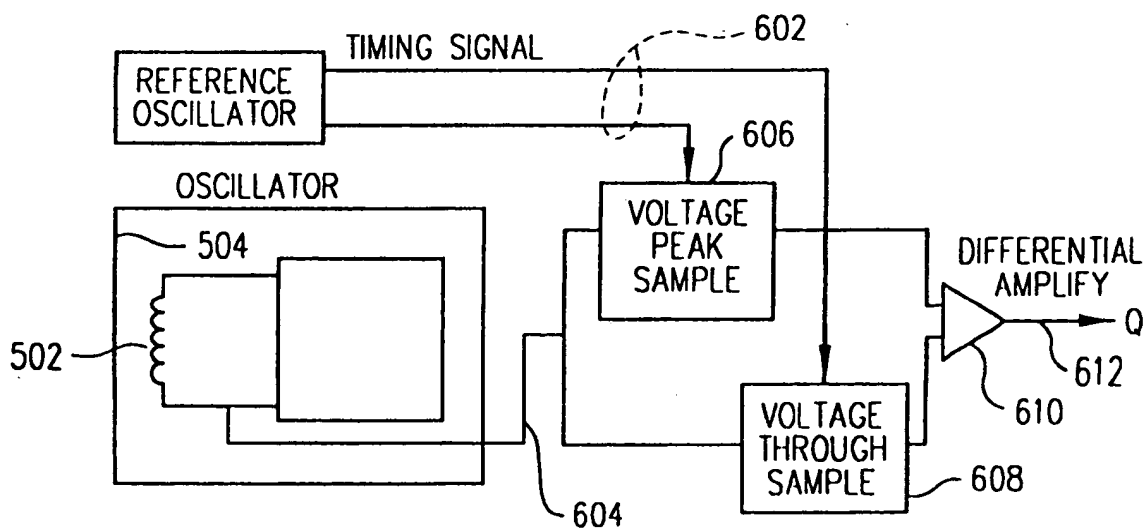


Fig. 6

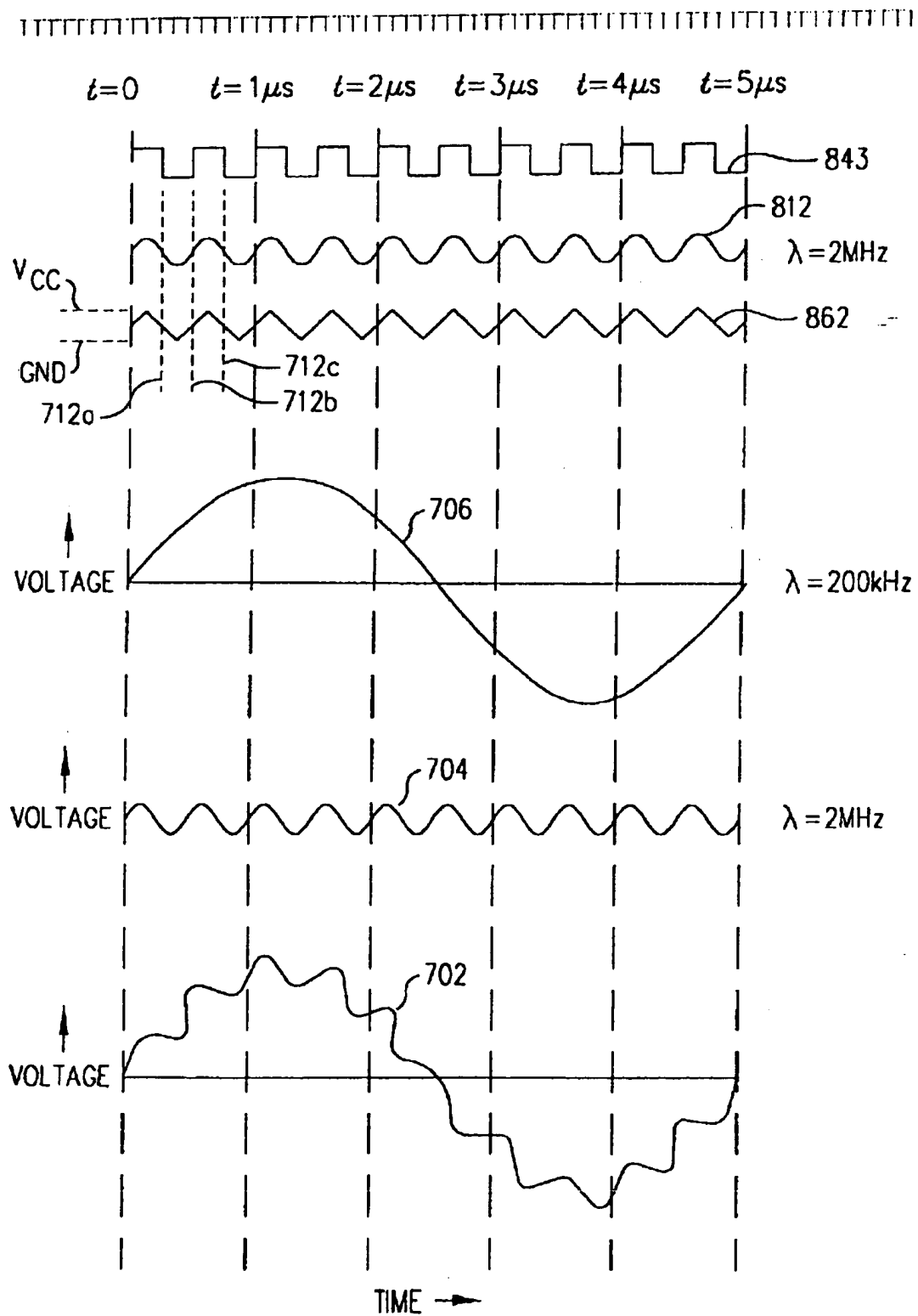


Fig. 7

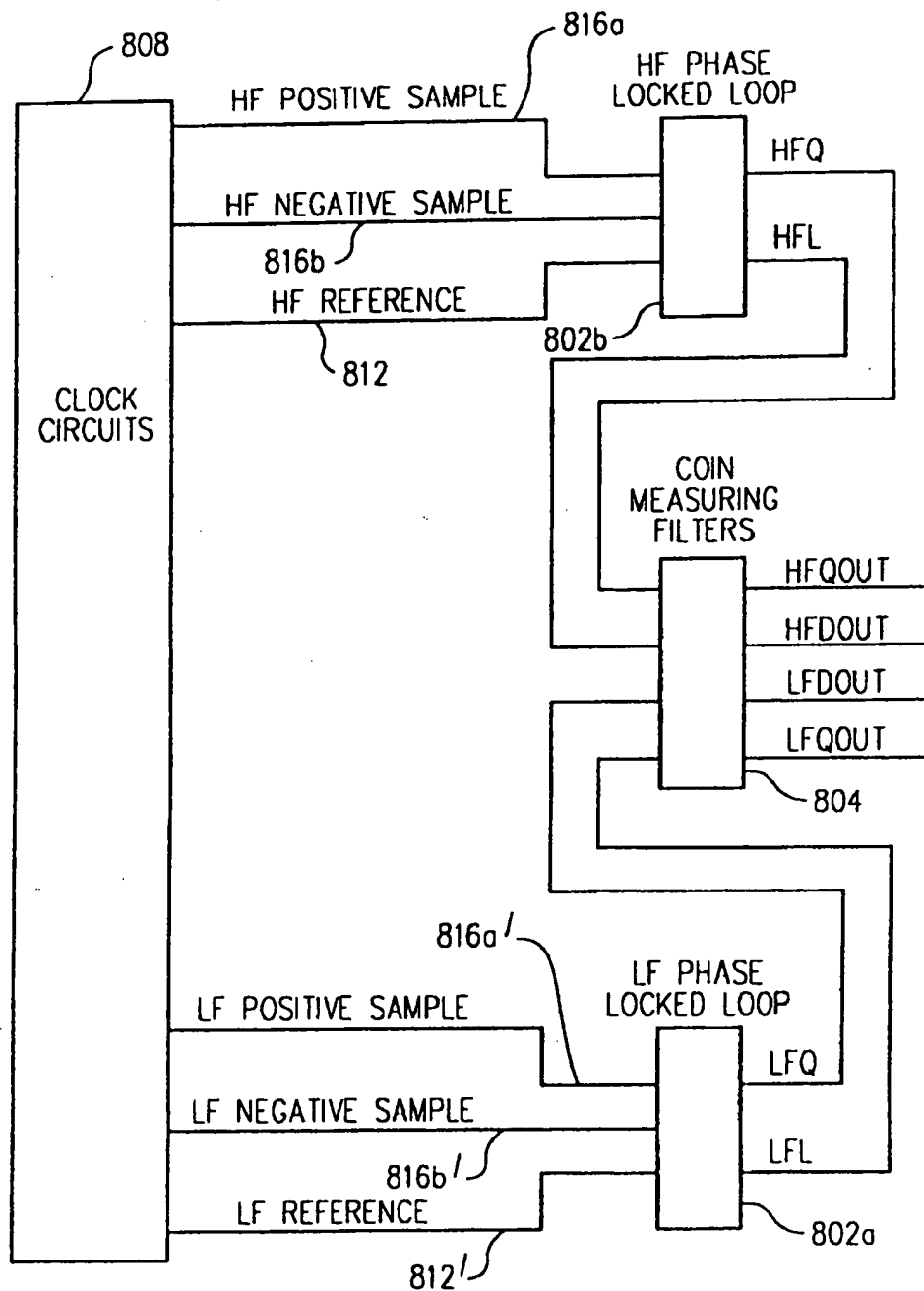


Fig. 8A

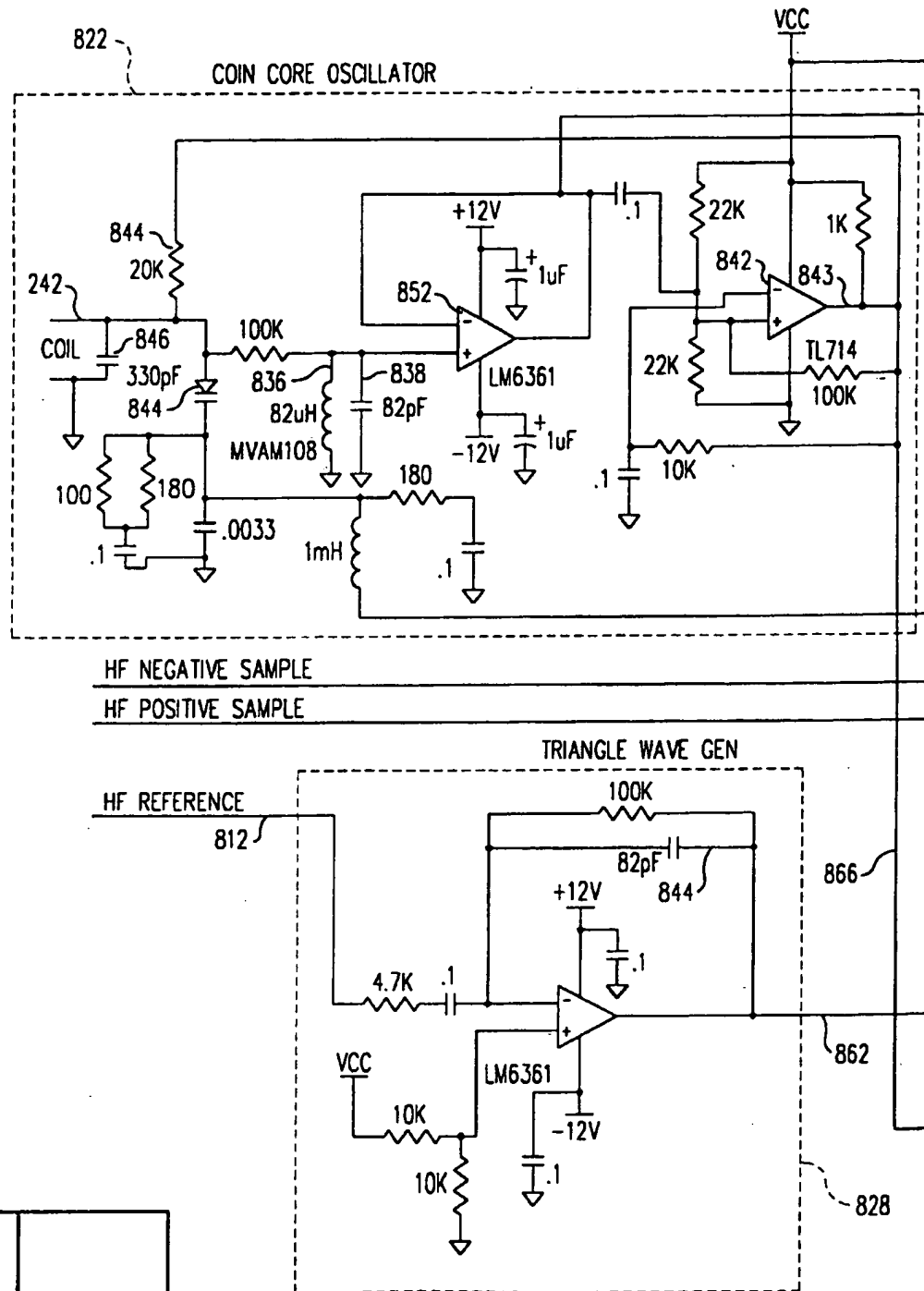


FIG. 8B-1	FIG. 8B-2
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Fig. 8B-1

Fig. 8B

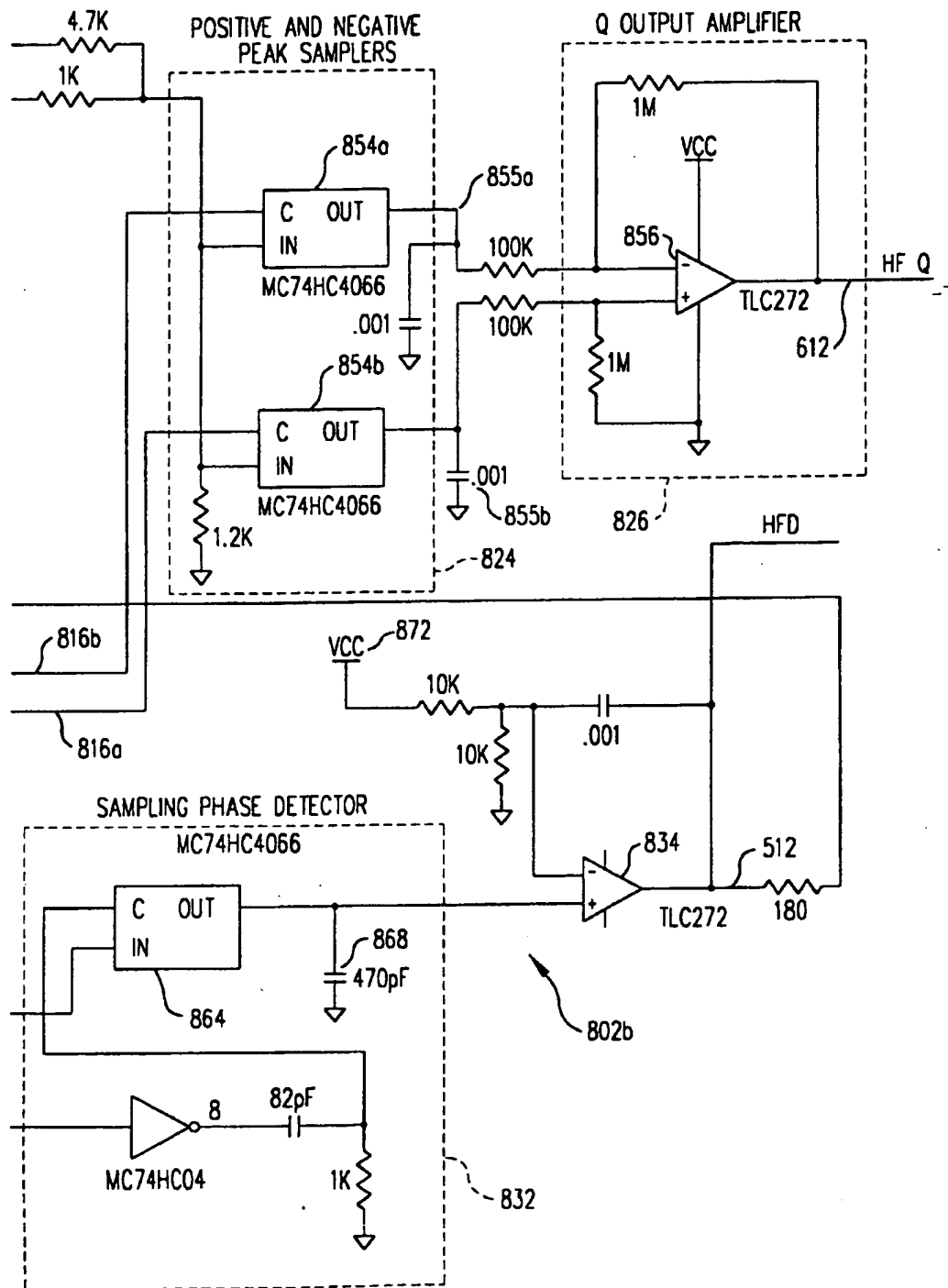


Fig. 8B-2

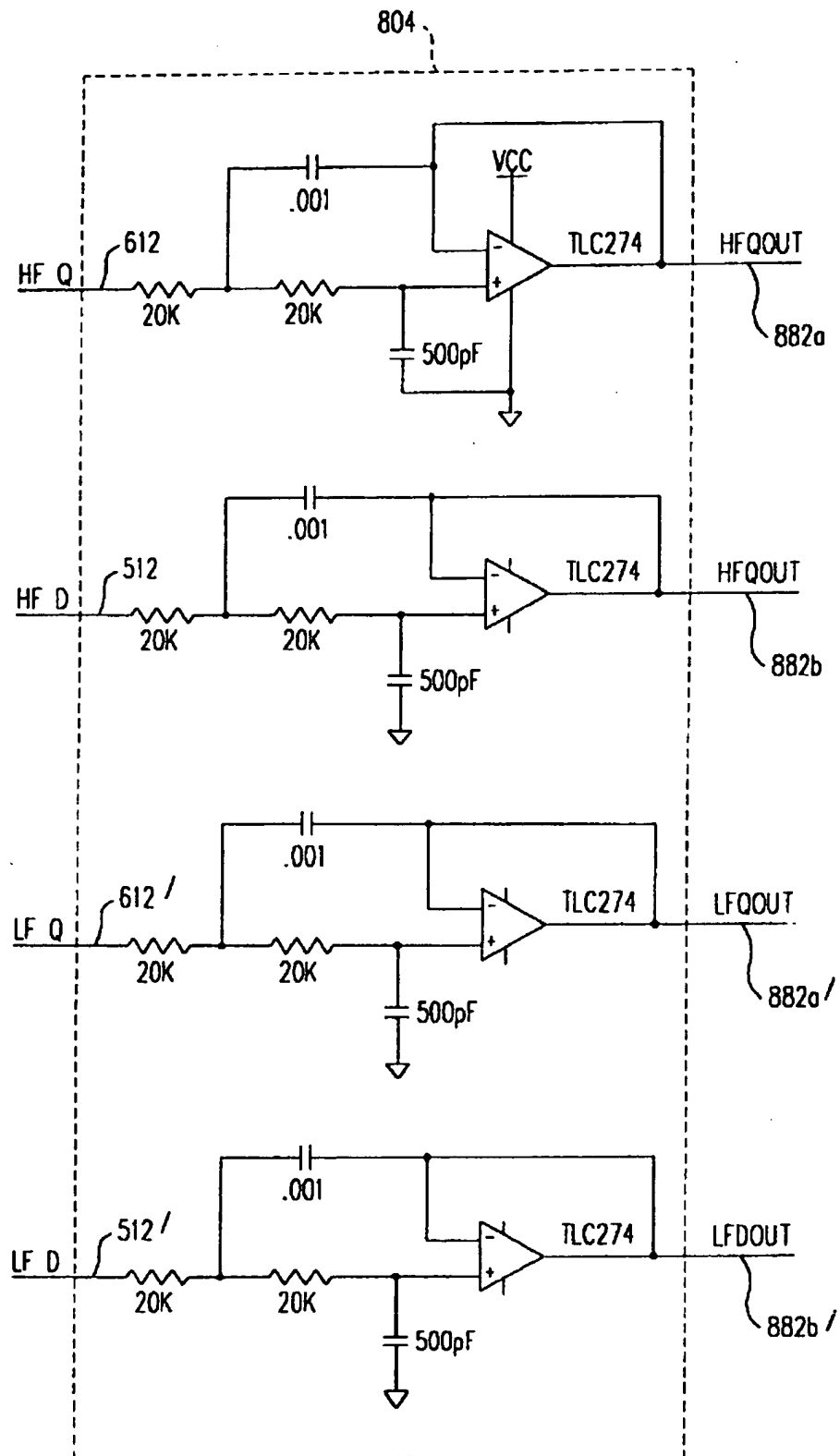


Fig. 8C

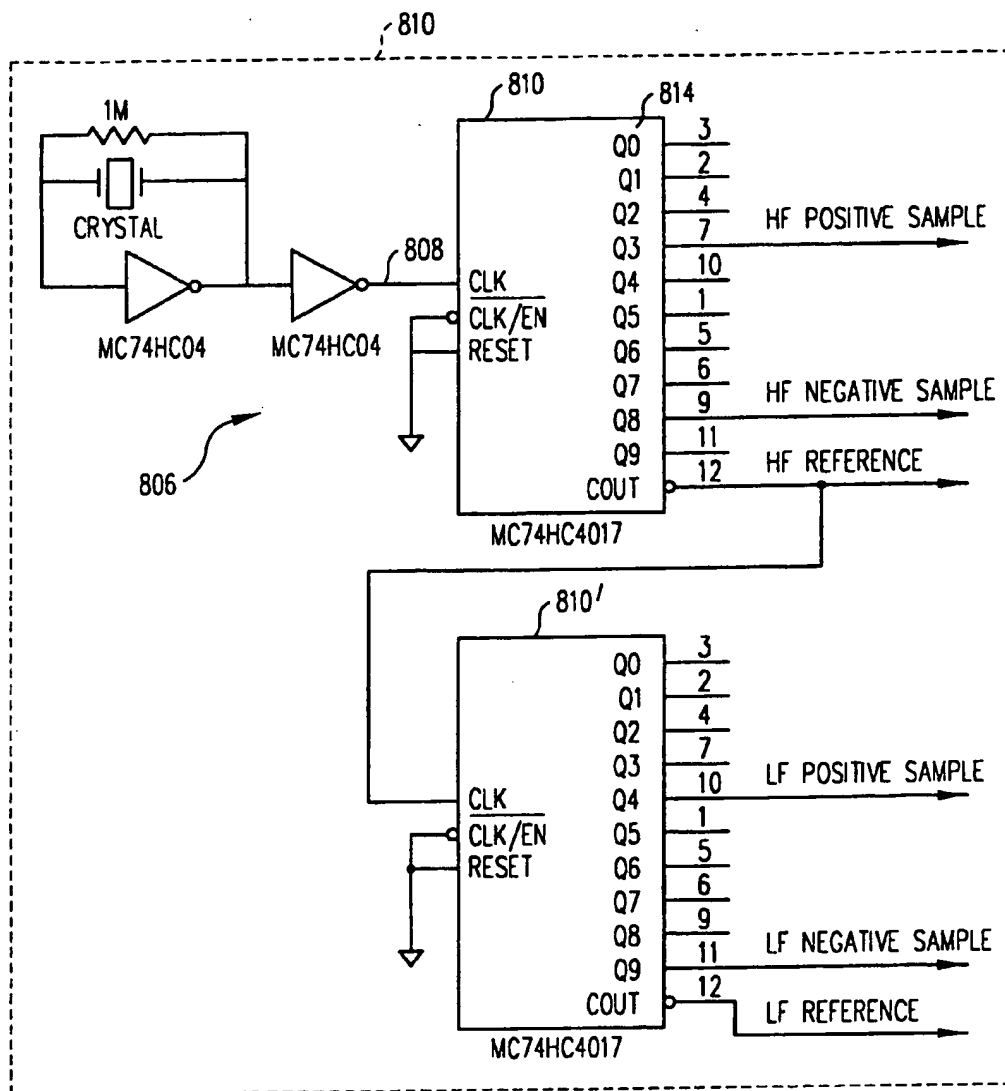


Fig. 8D

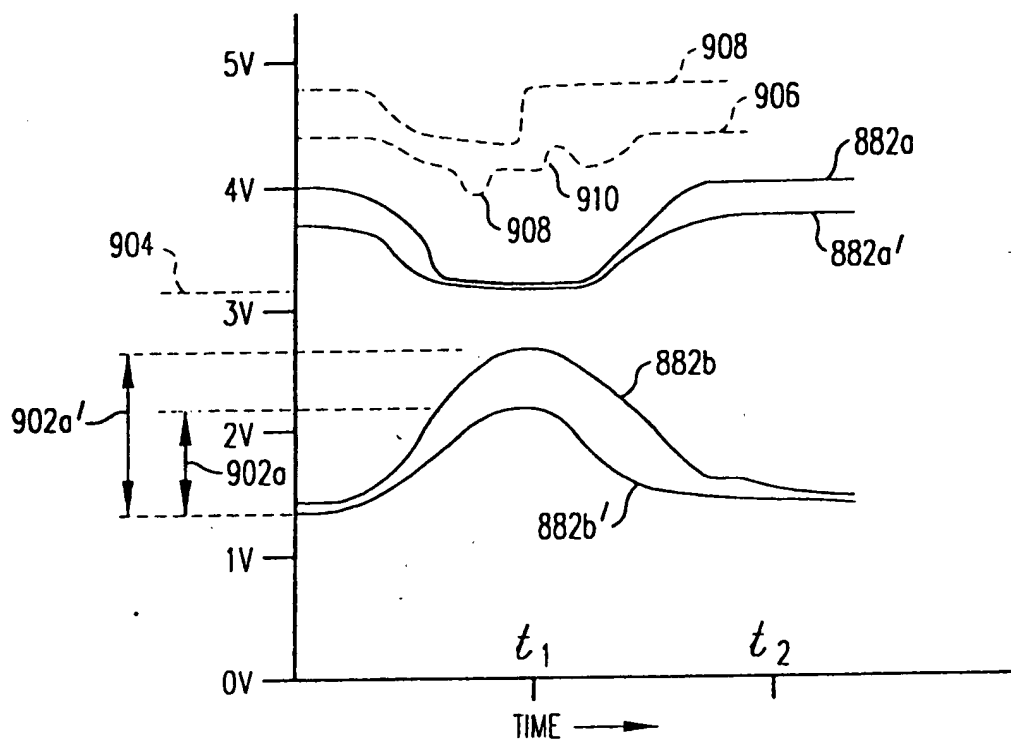


Fig. 9

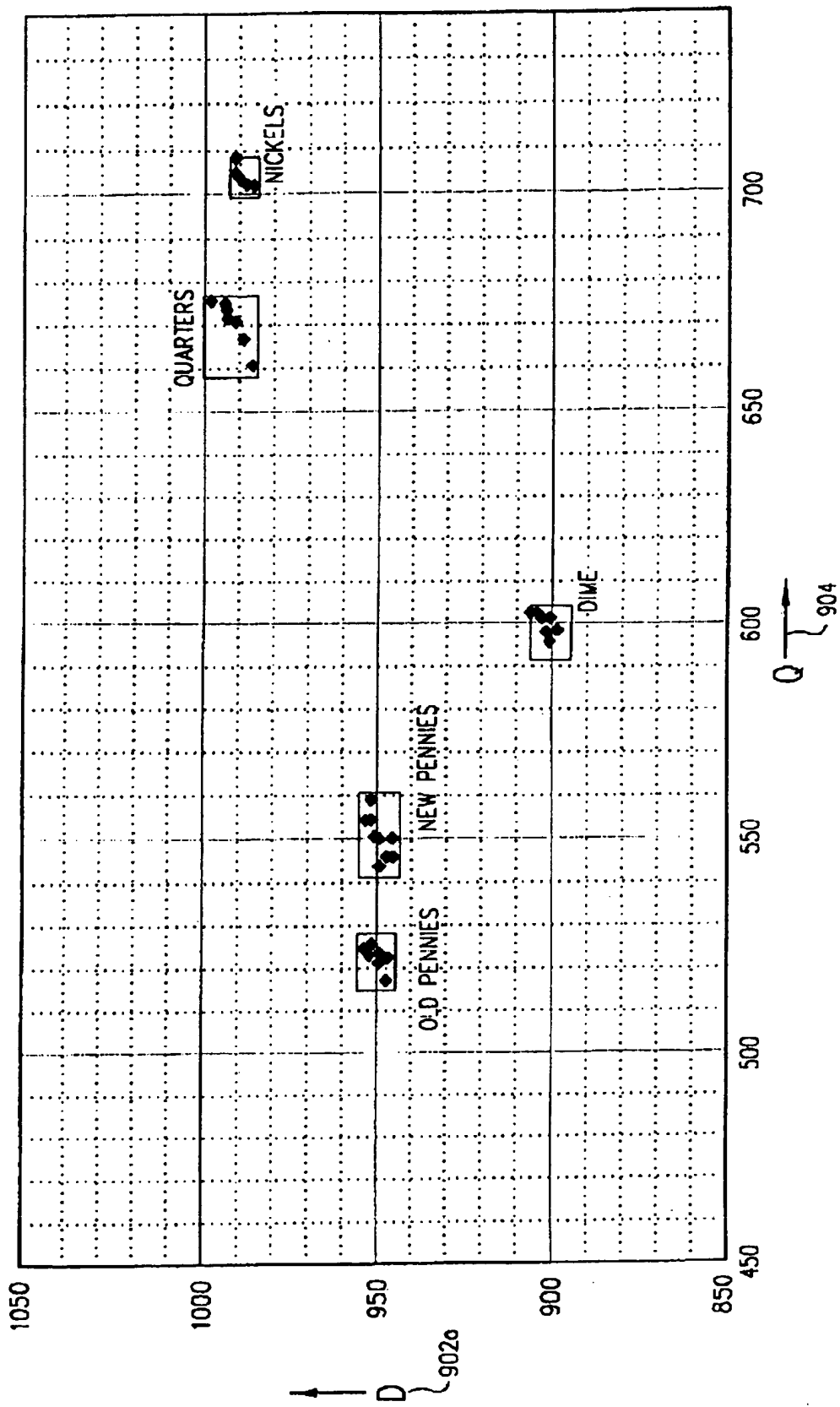


Fig. 10A

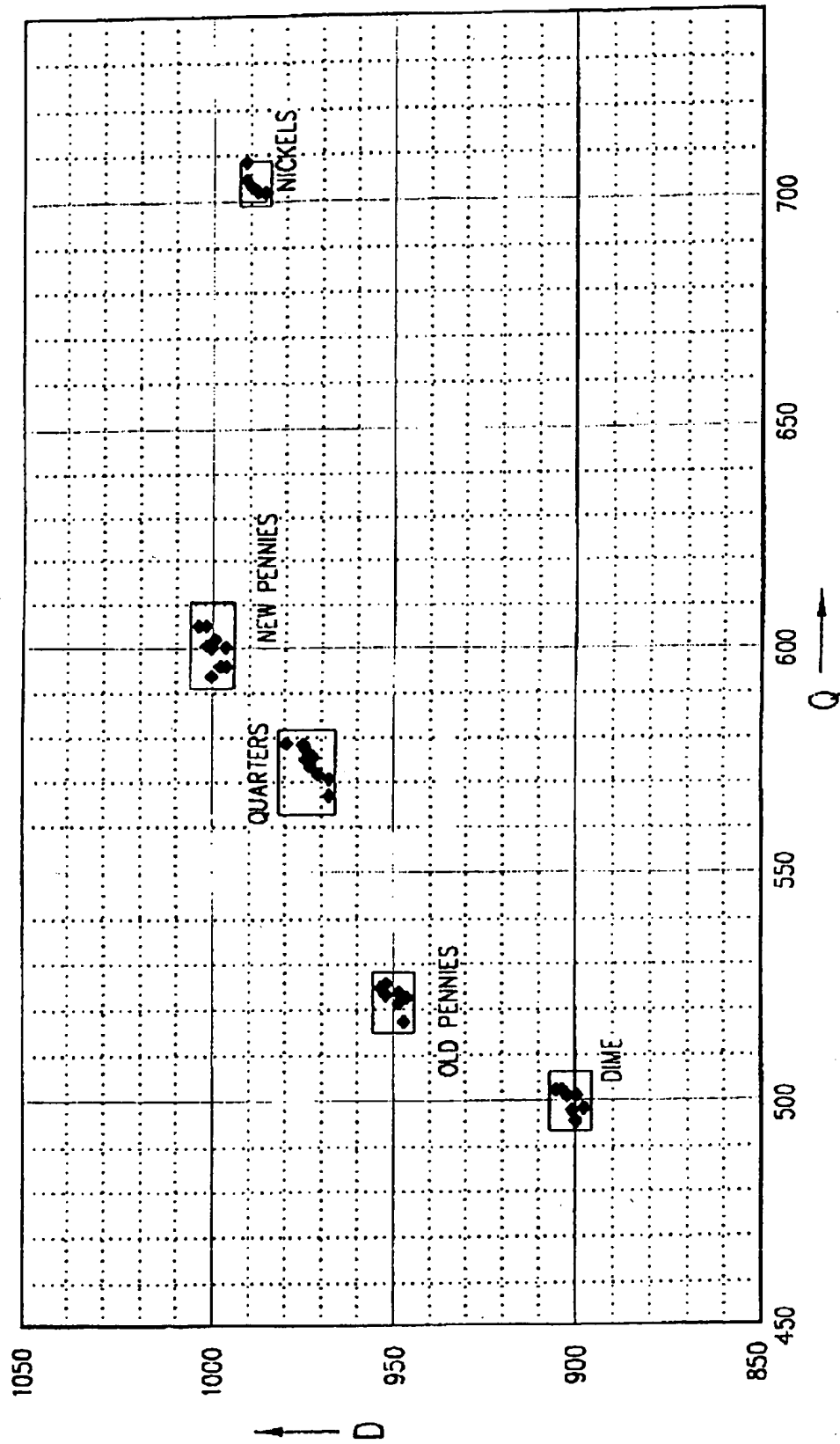


Fig. 10B

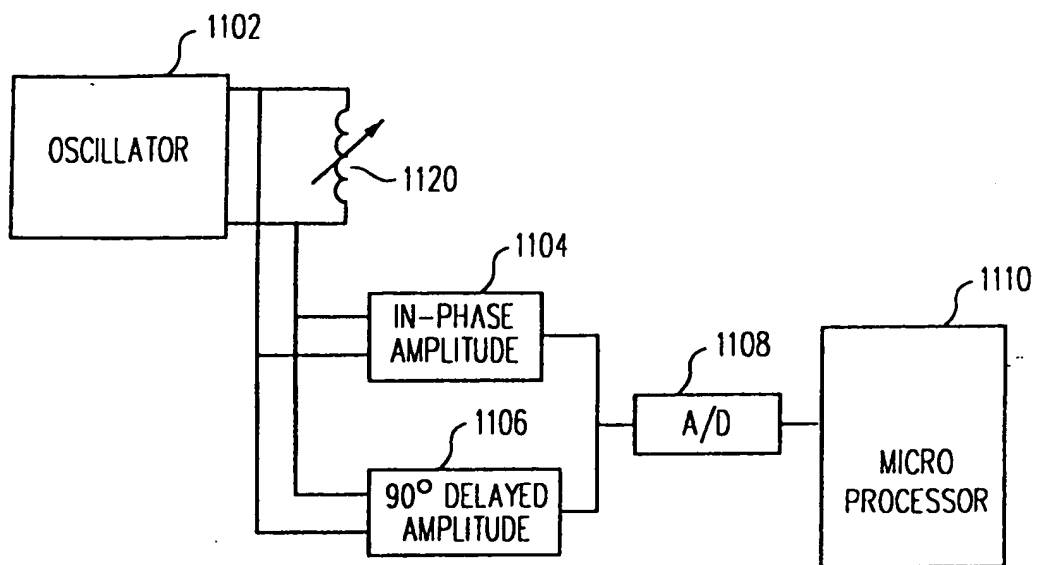


Fig. 11

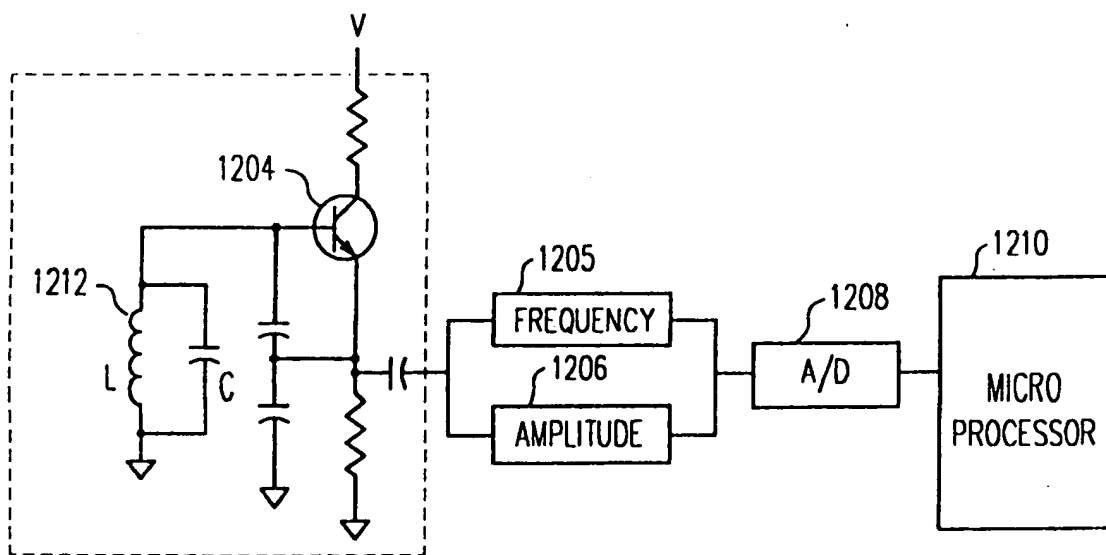


Fig. 12

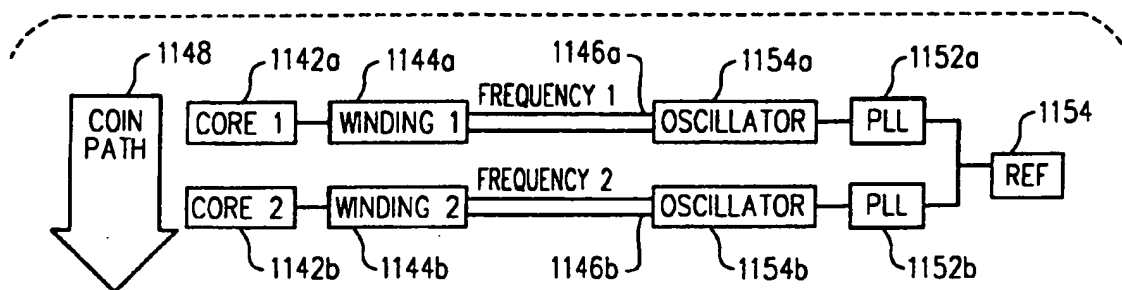


Fig. 11A

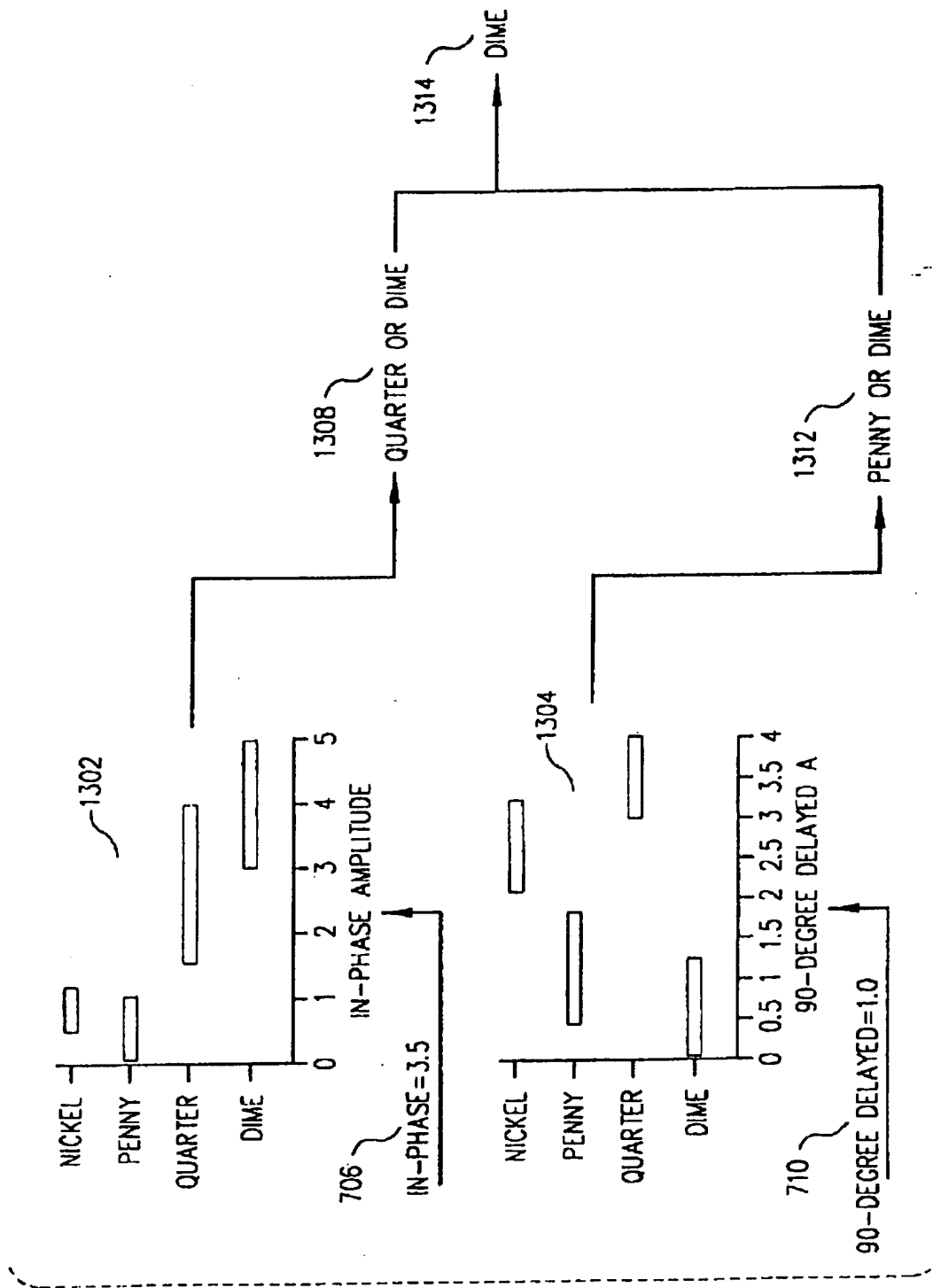


Fig. 13

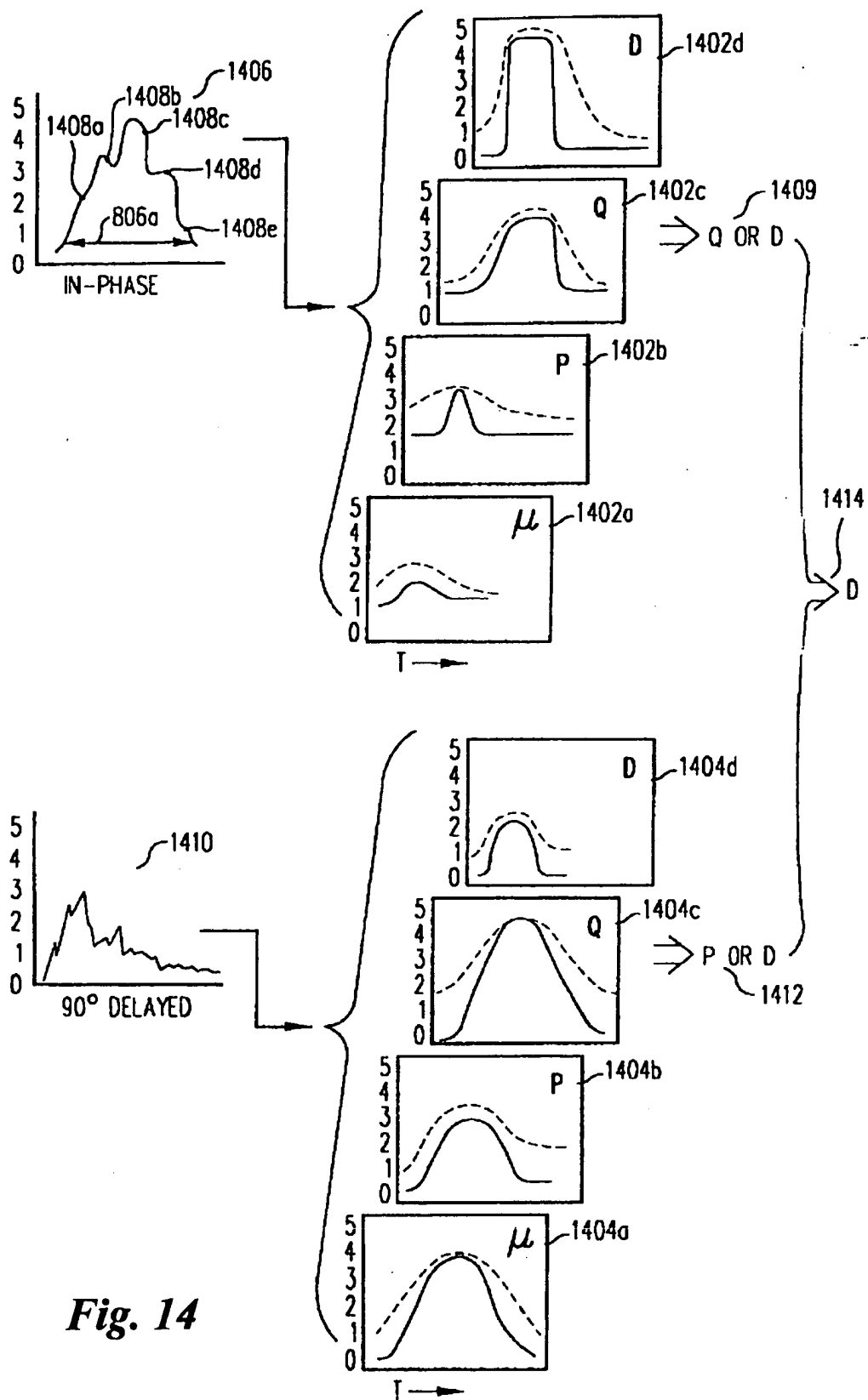


Fig. 14

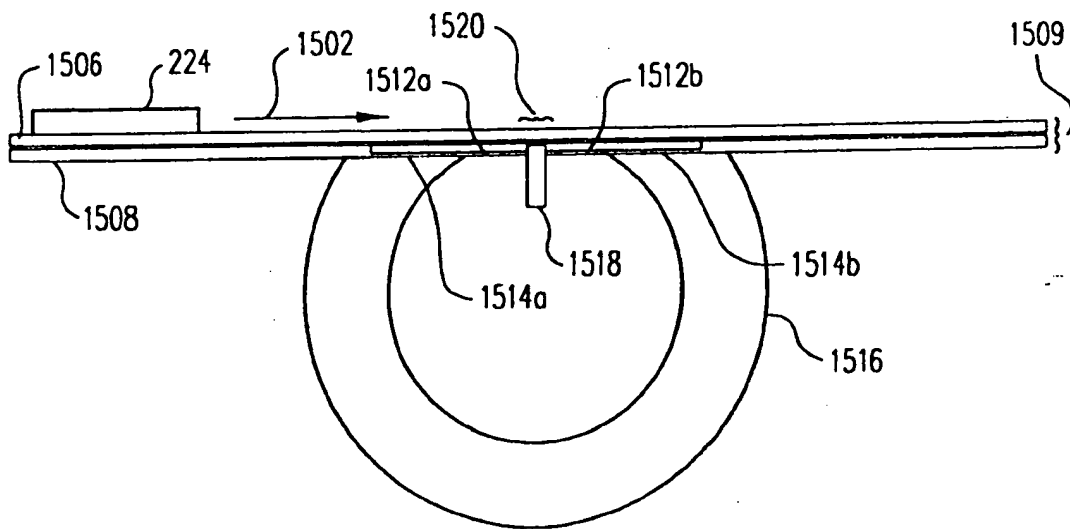


Fig. 15A

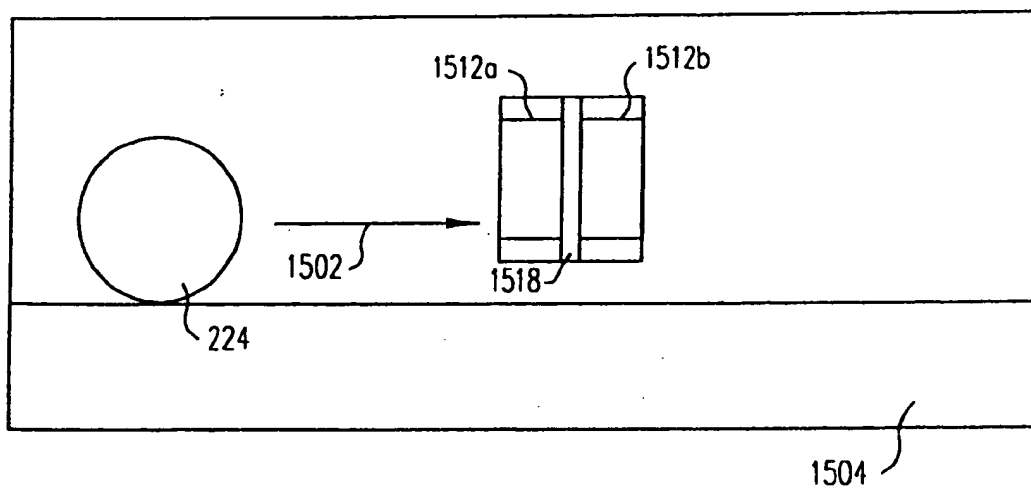


Fig. 15B

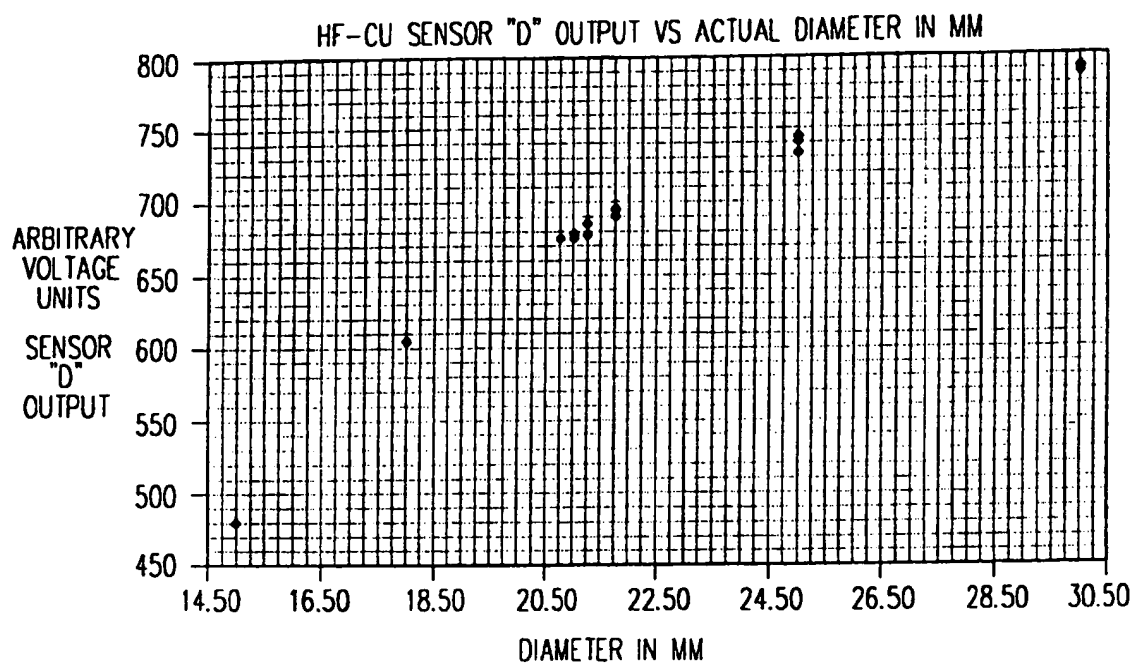


Fig. 16A

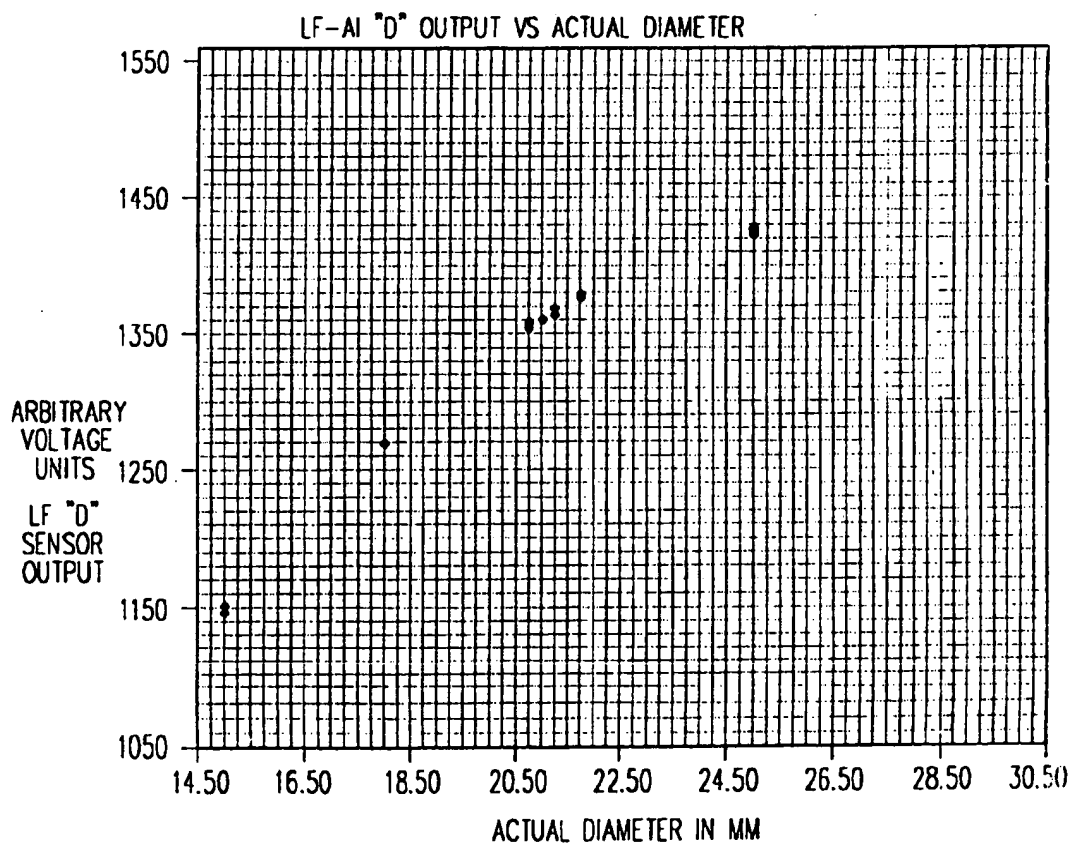


Fig. 16B

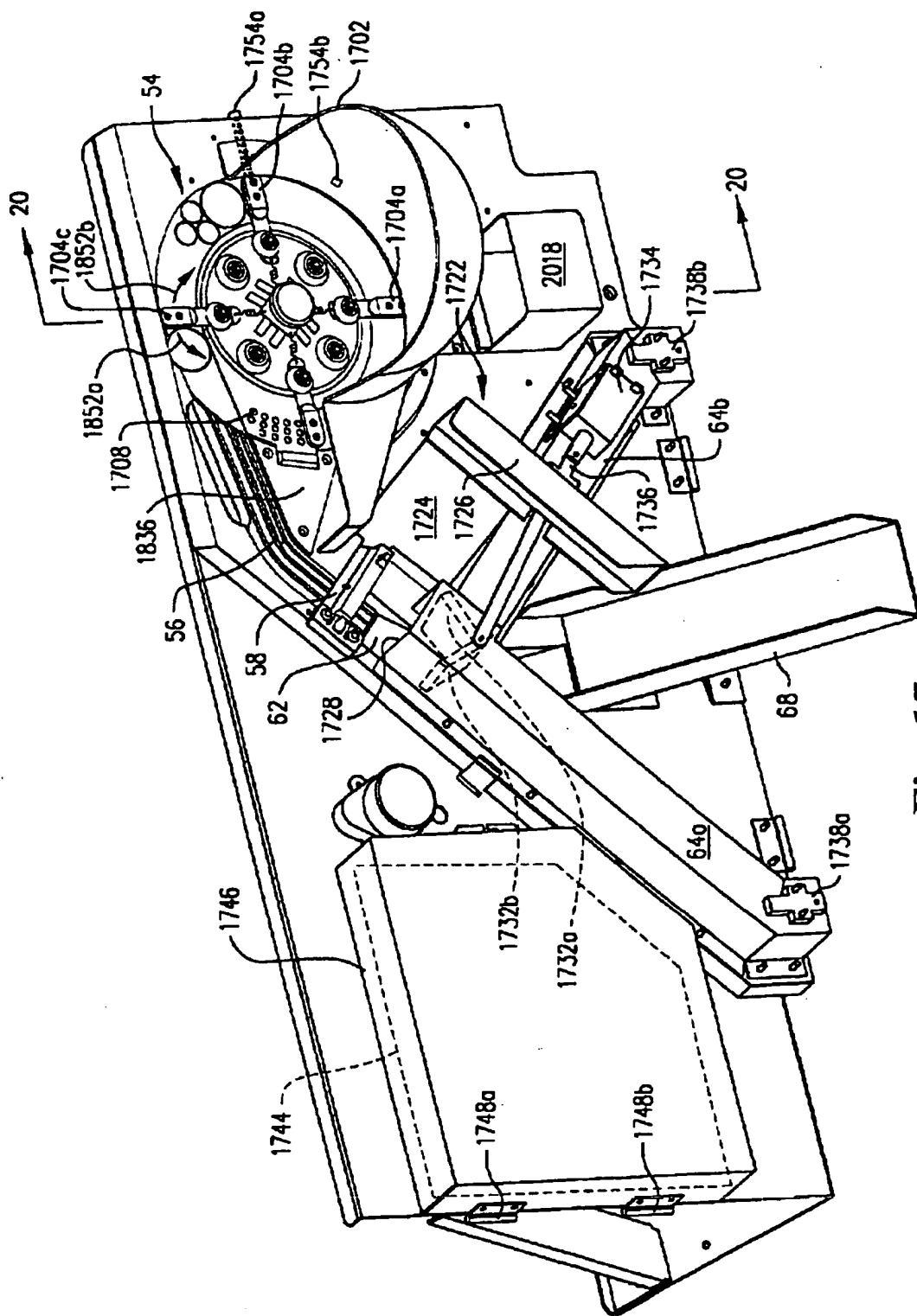


Fig. 17

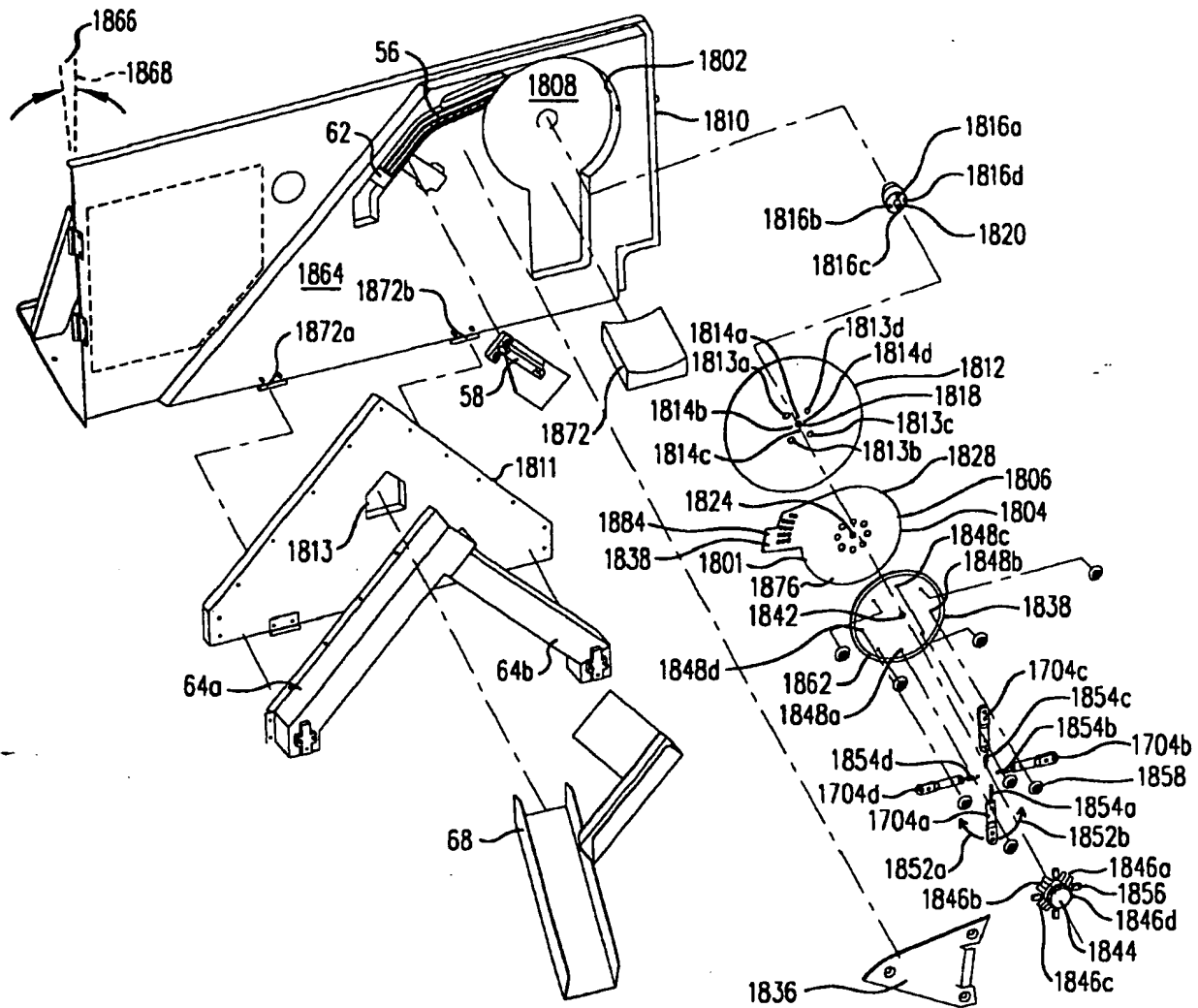


Fig. 18

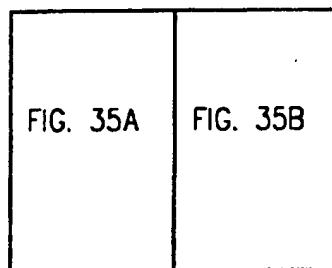


Fig. 35

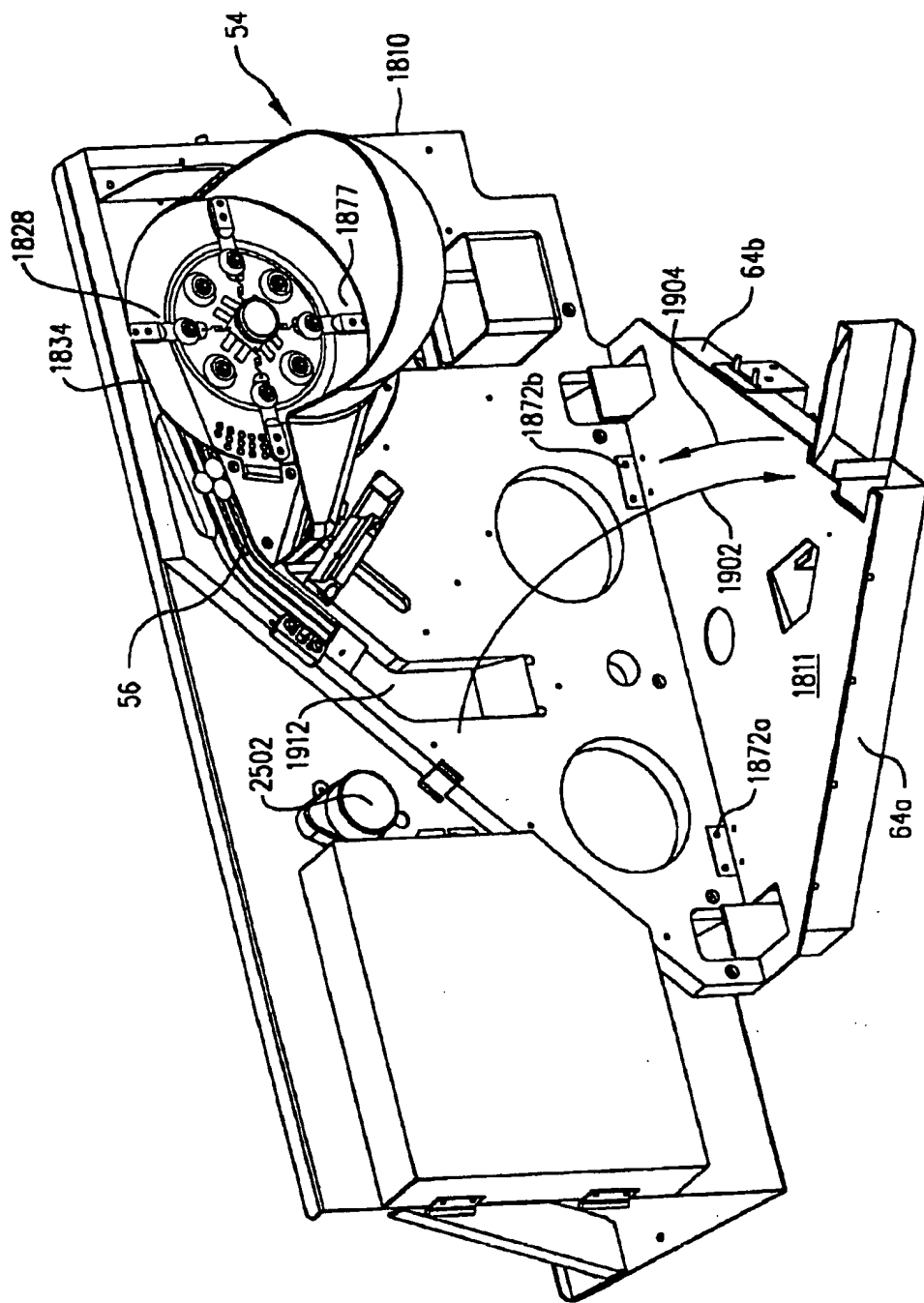


Fig. 19

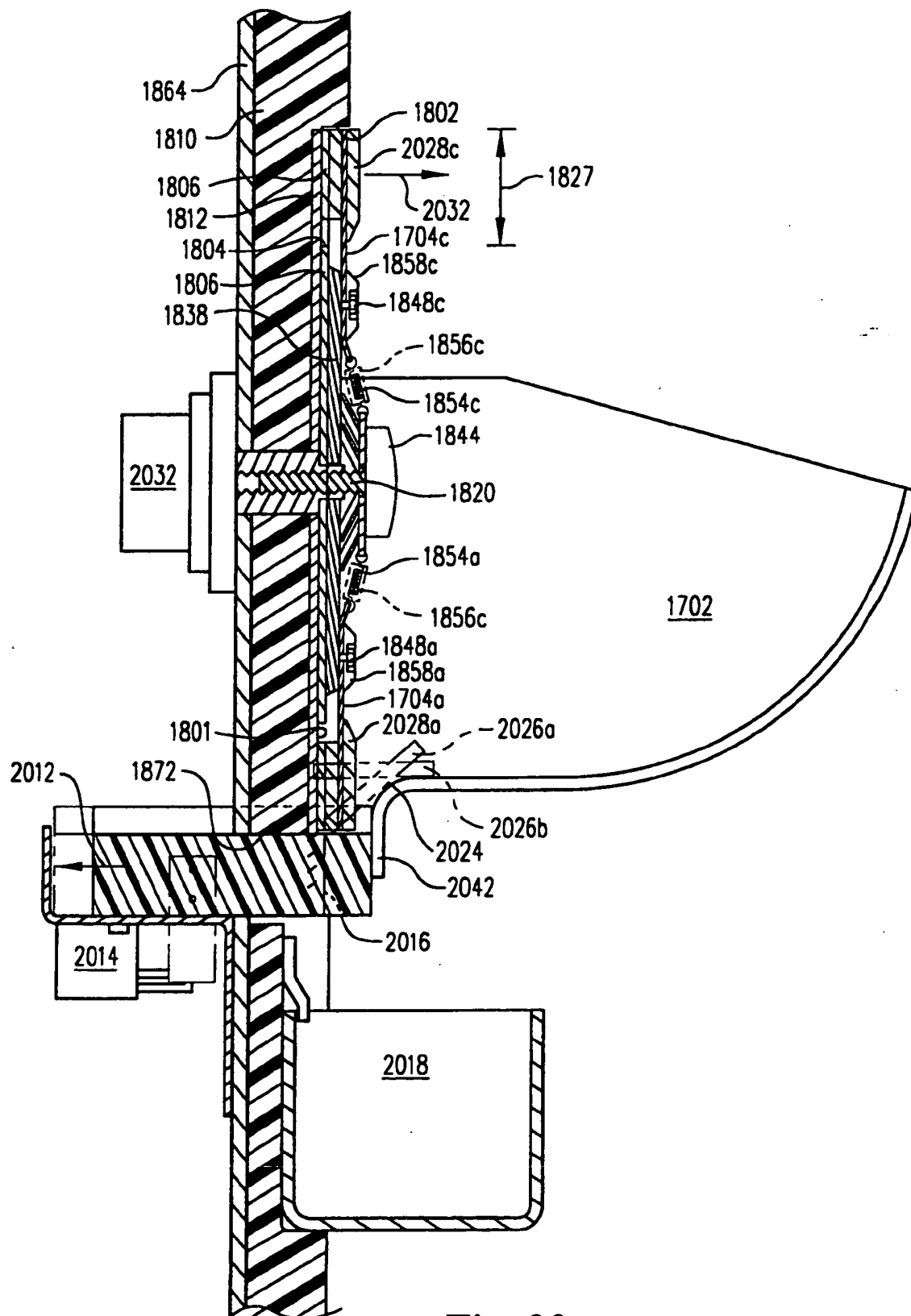


Fig. 20

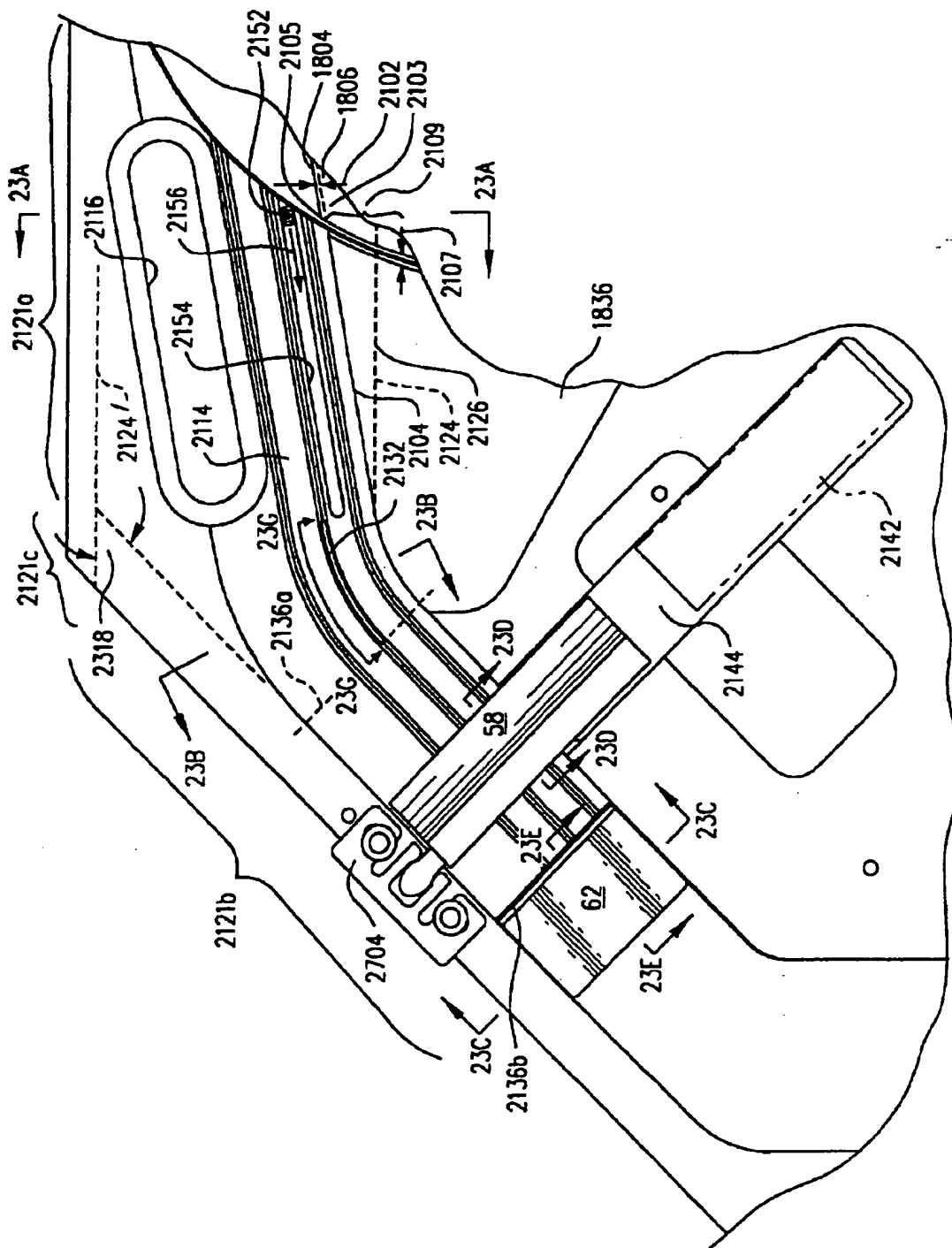


Fig. 21

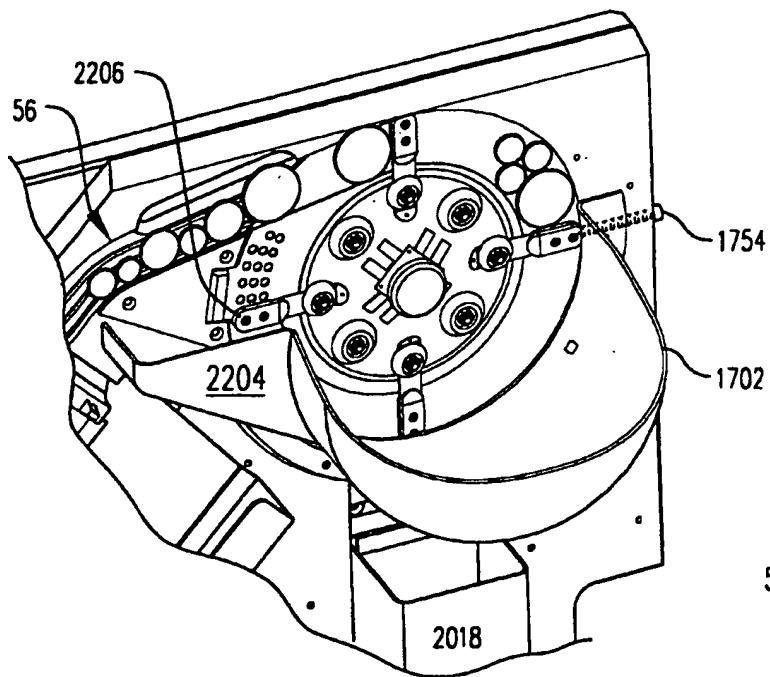
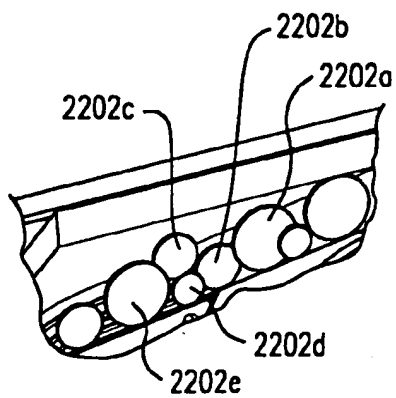


Fig. 22



22A

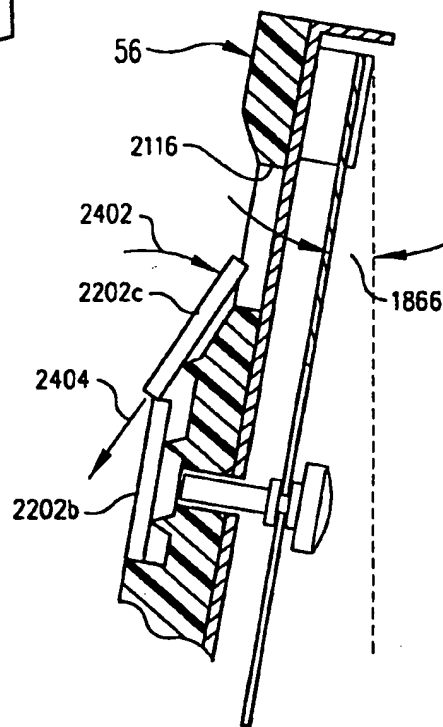


Fig. 24

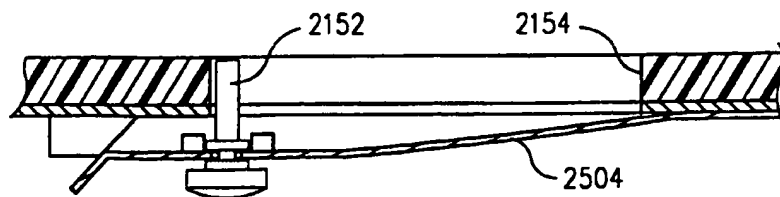


Fig. 26

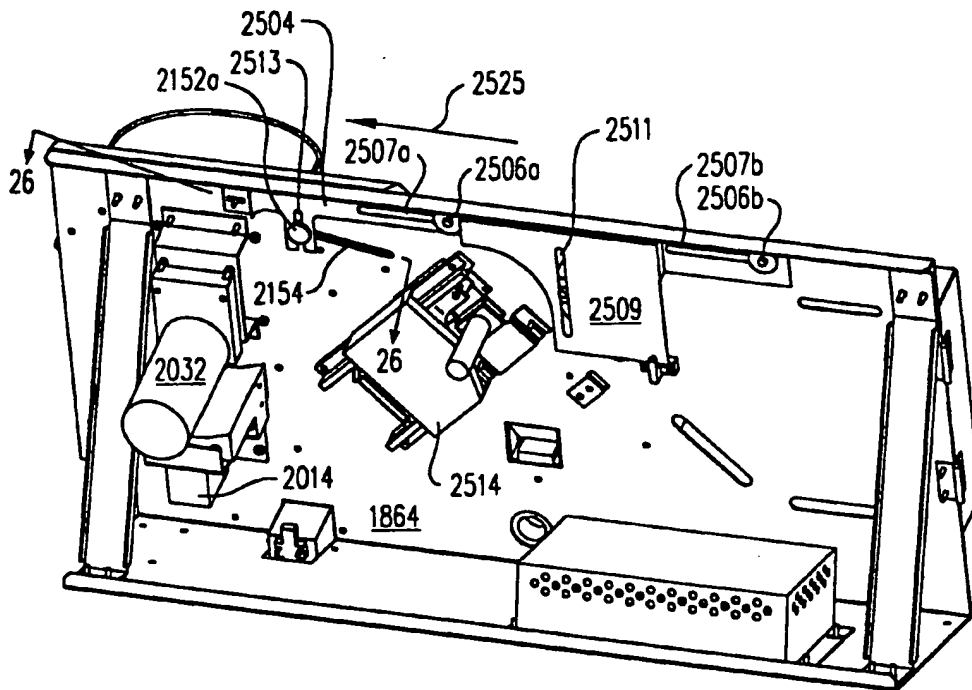


Fig. 25

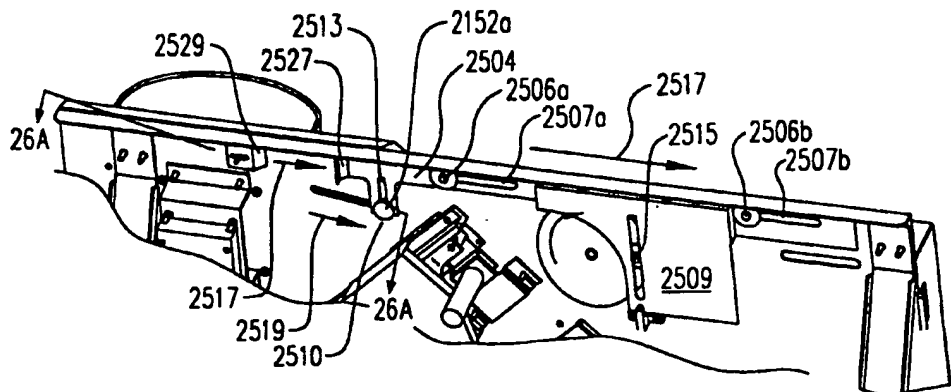


Fig. 25A

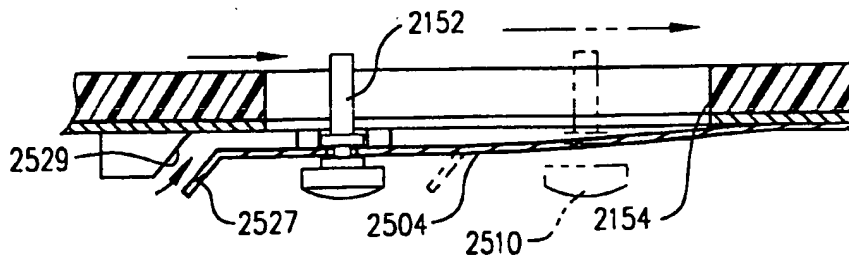


Fig. 26A

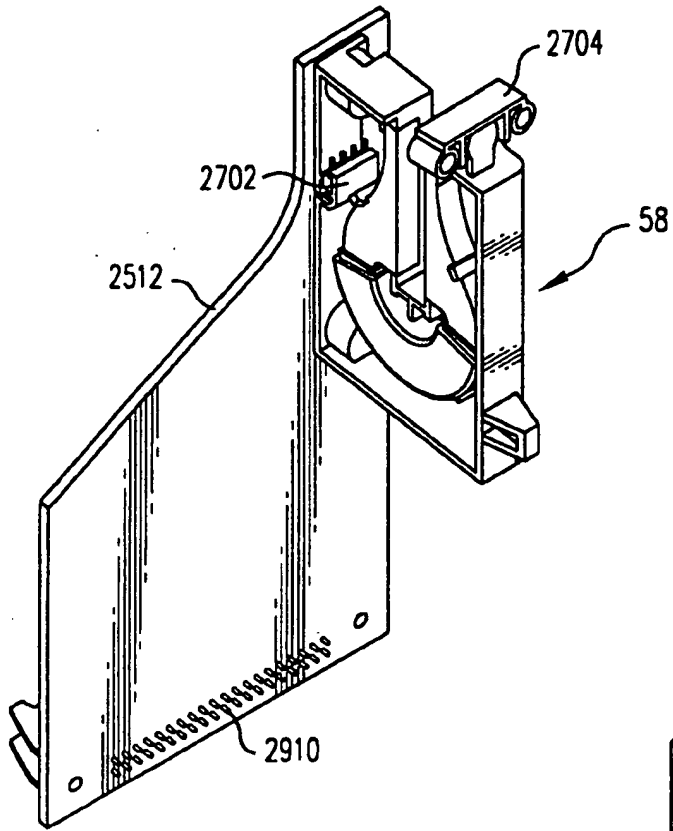


Fig. 27A

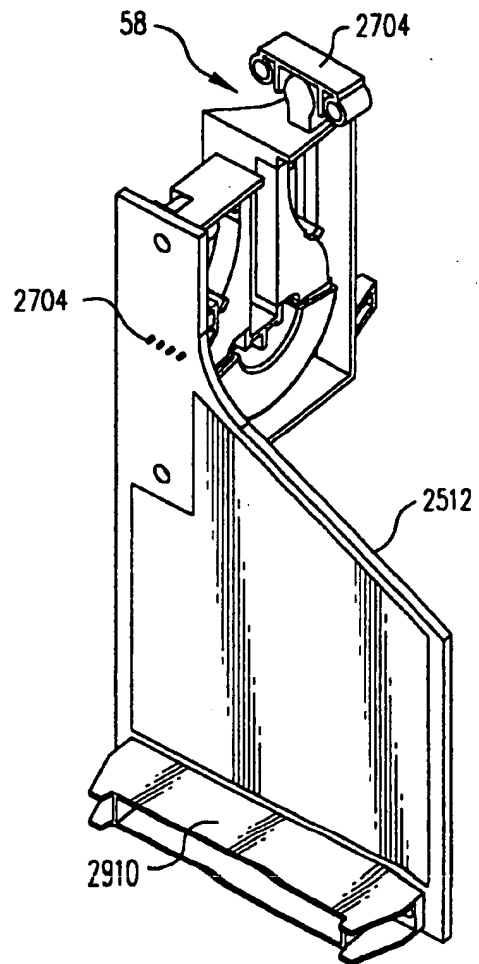


Fig. 27B

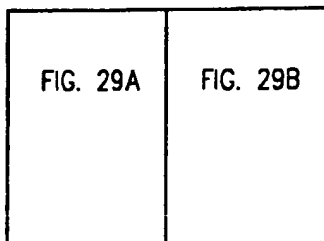


Fig. 29

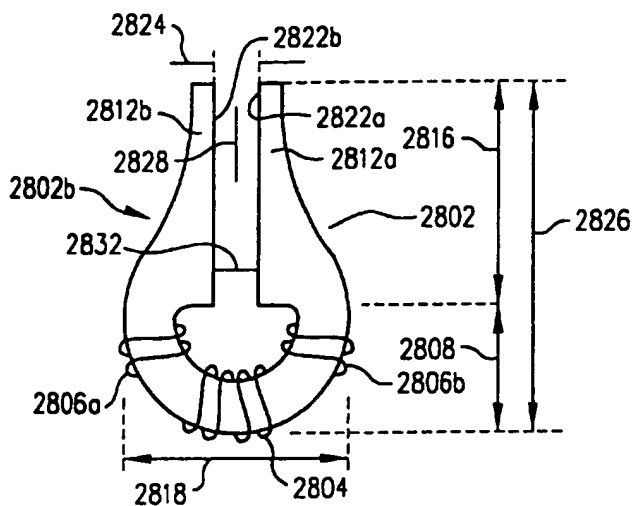


Fig. 28A

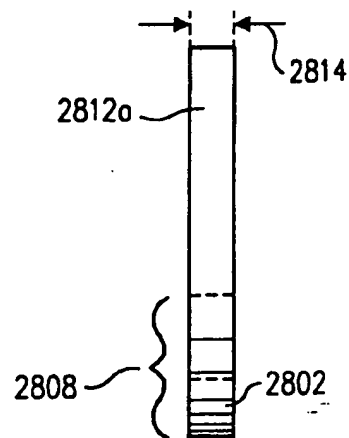


Fig. 28B

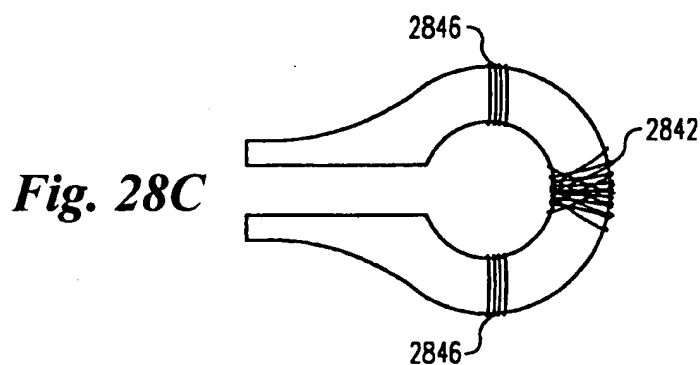


Fig. 28C

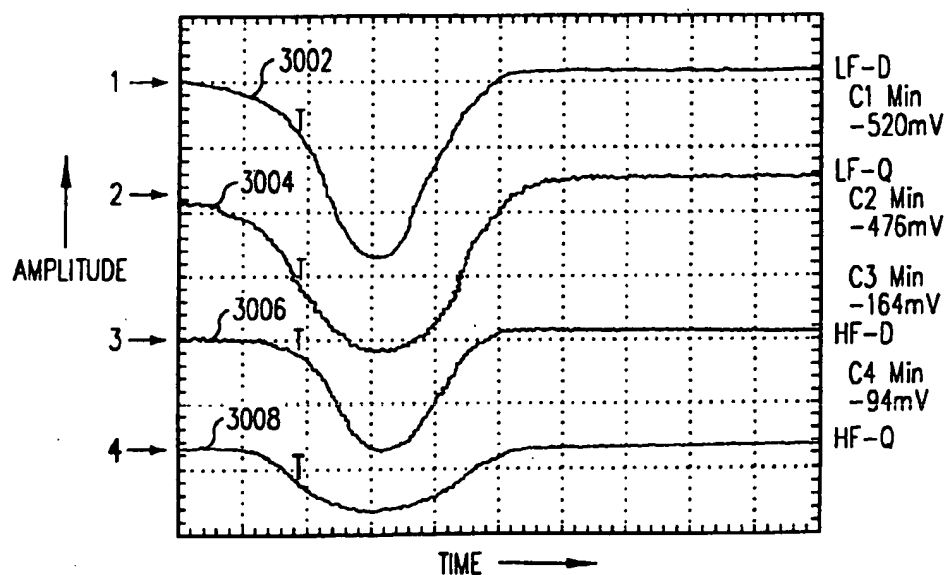


Fig. 30

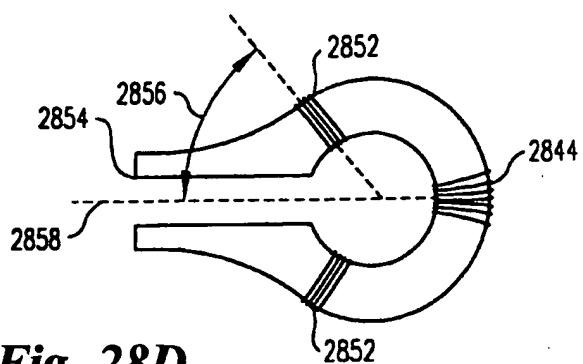


Fig. 28D

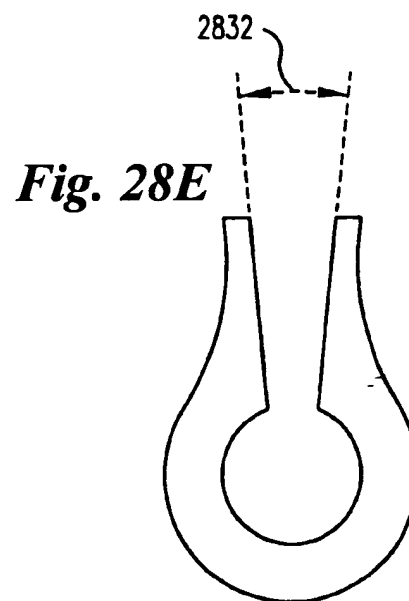


Fig. 28E

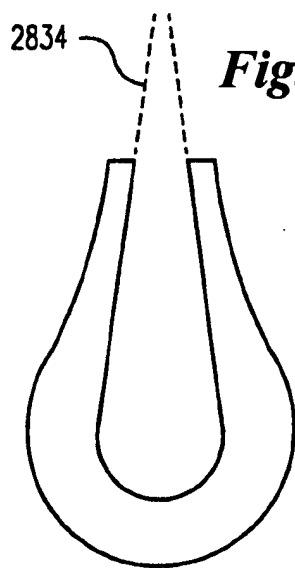


Fig. 28F



Fig. 28G

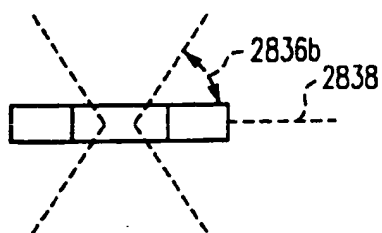


Fig. 28H



Fig. 28I

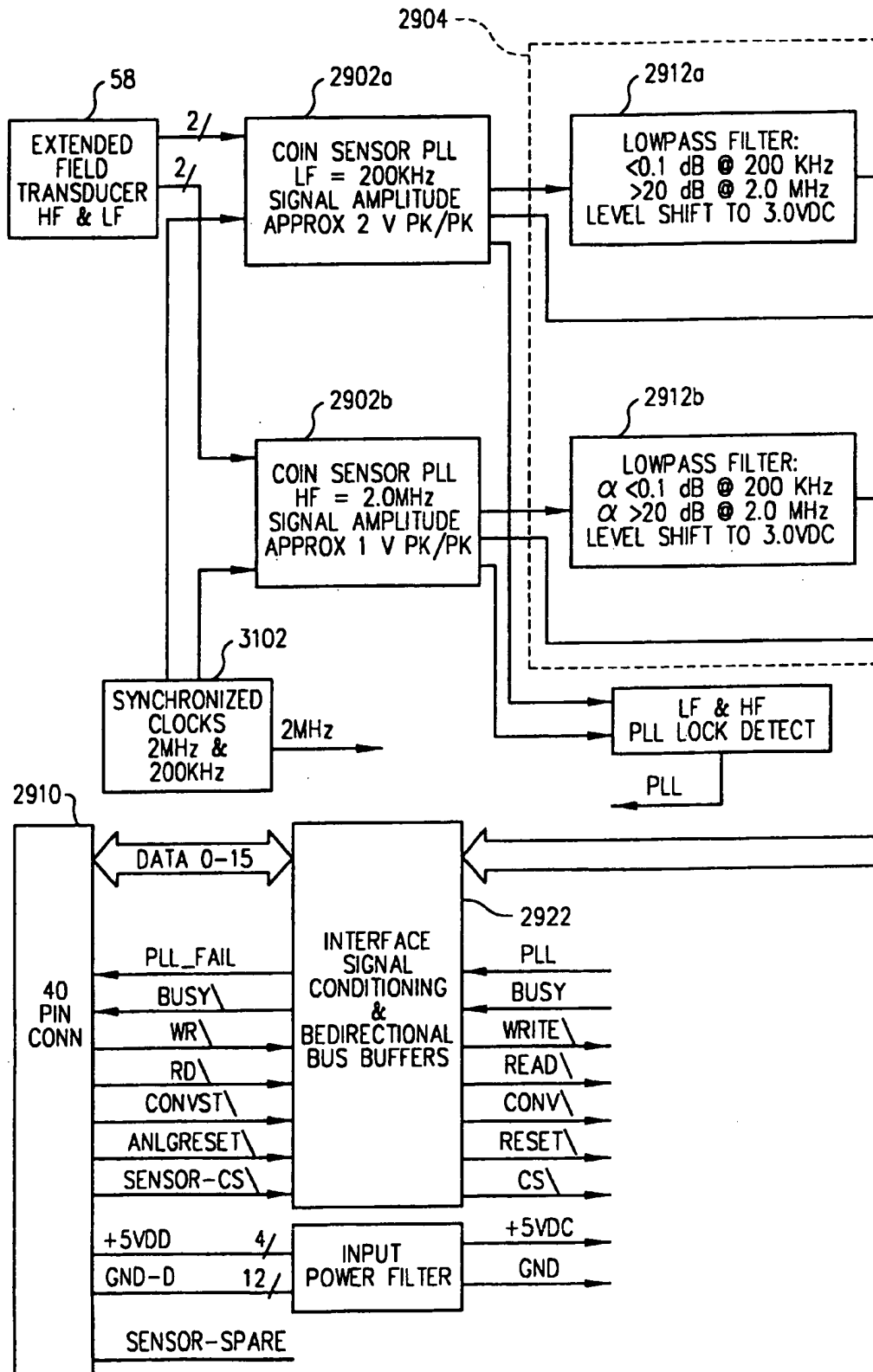


Fig. 29A

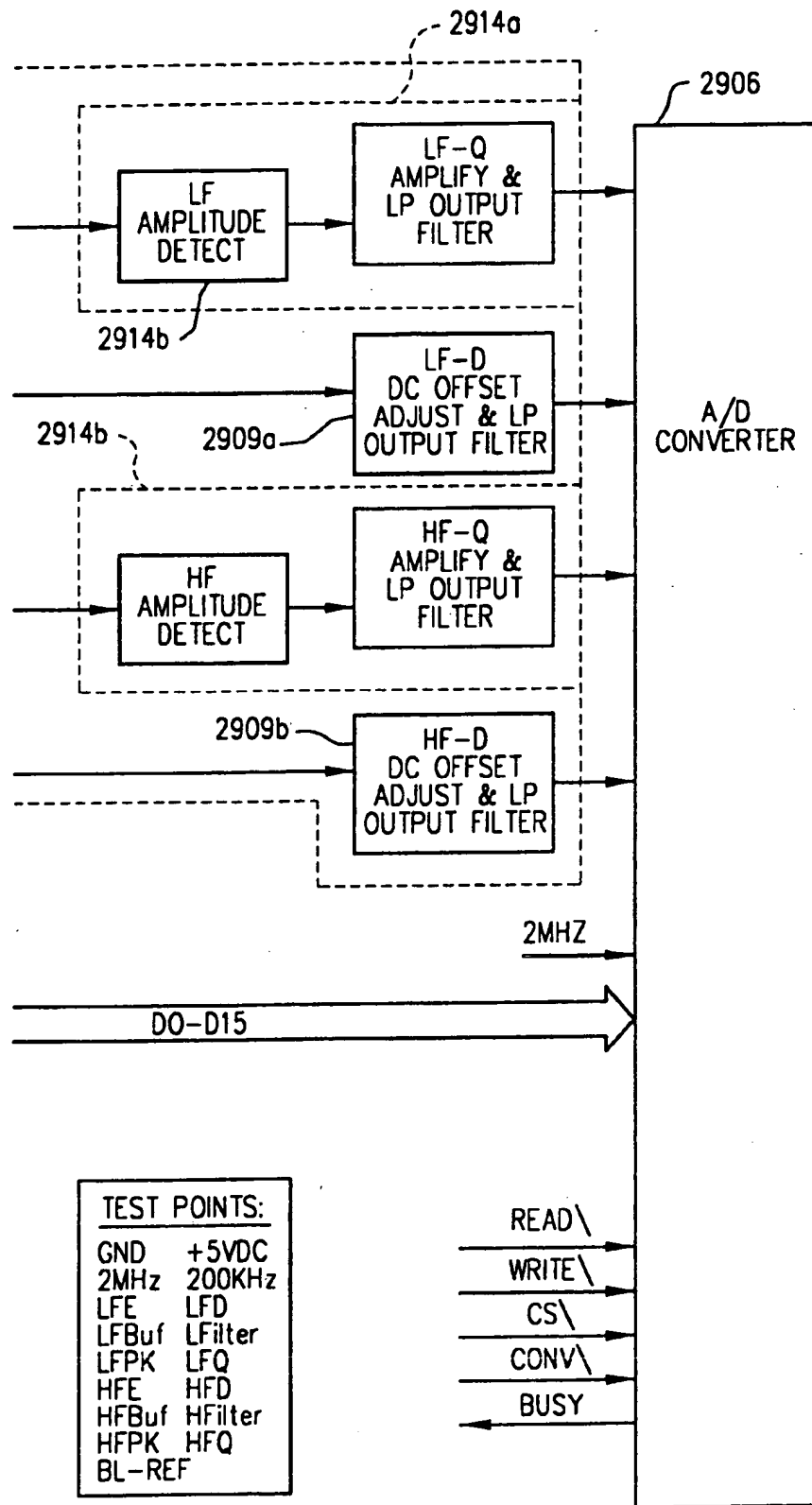


Fig. 29B

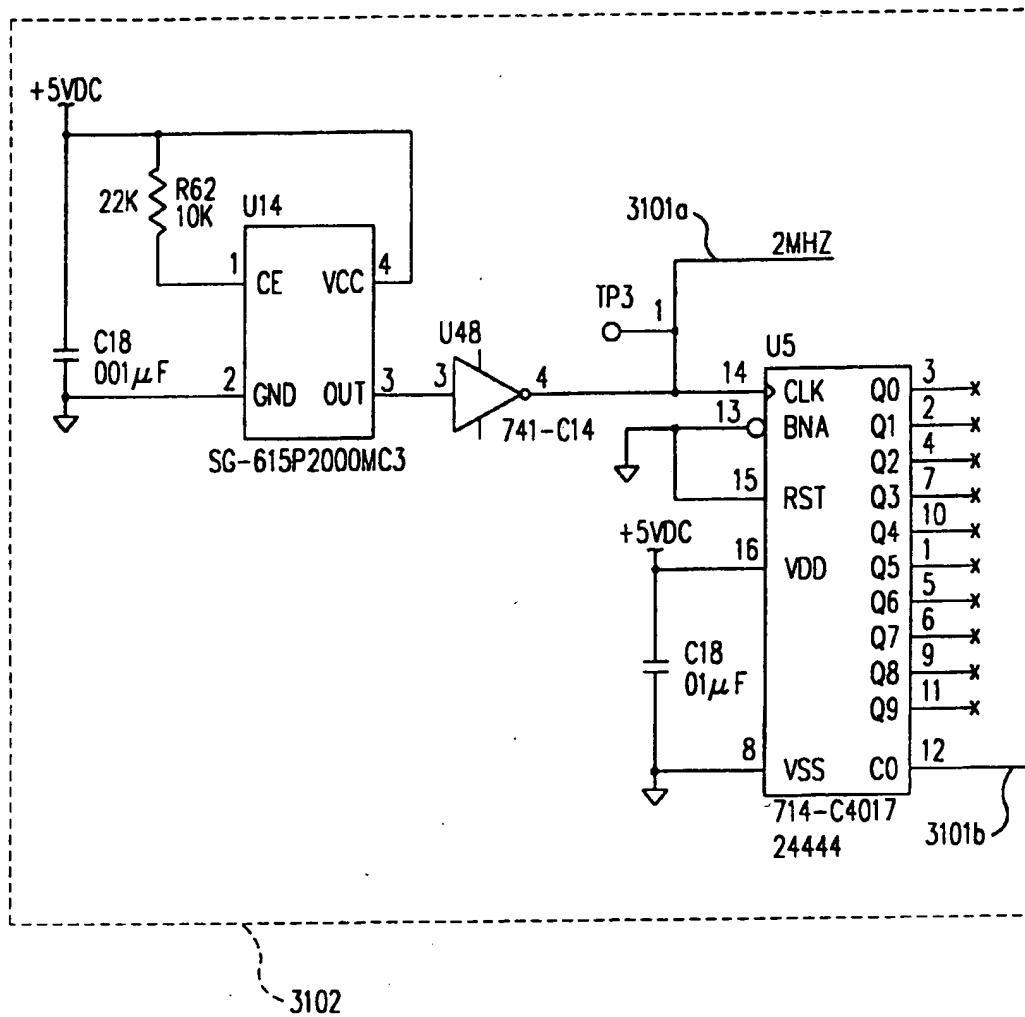


Fig. 31A

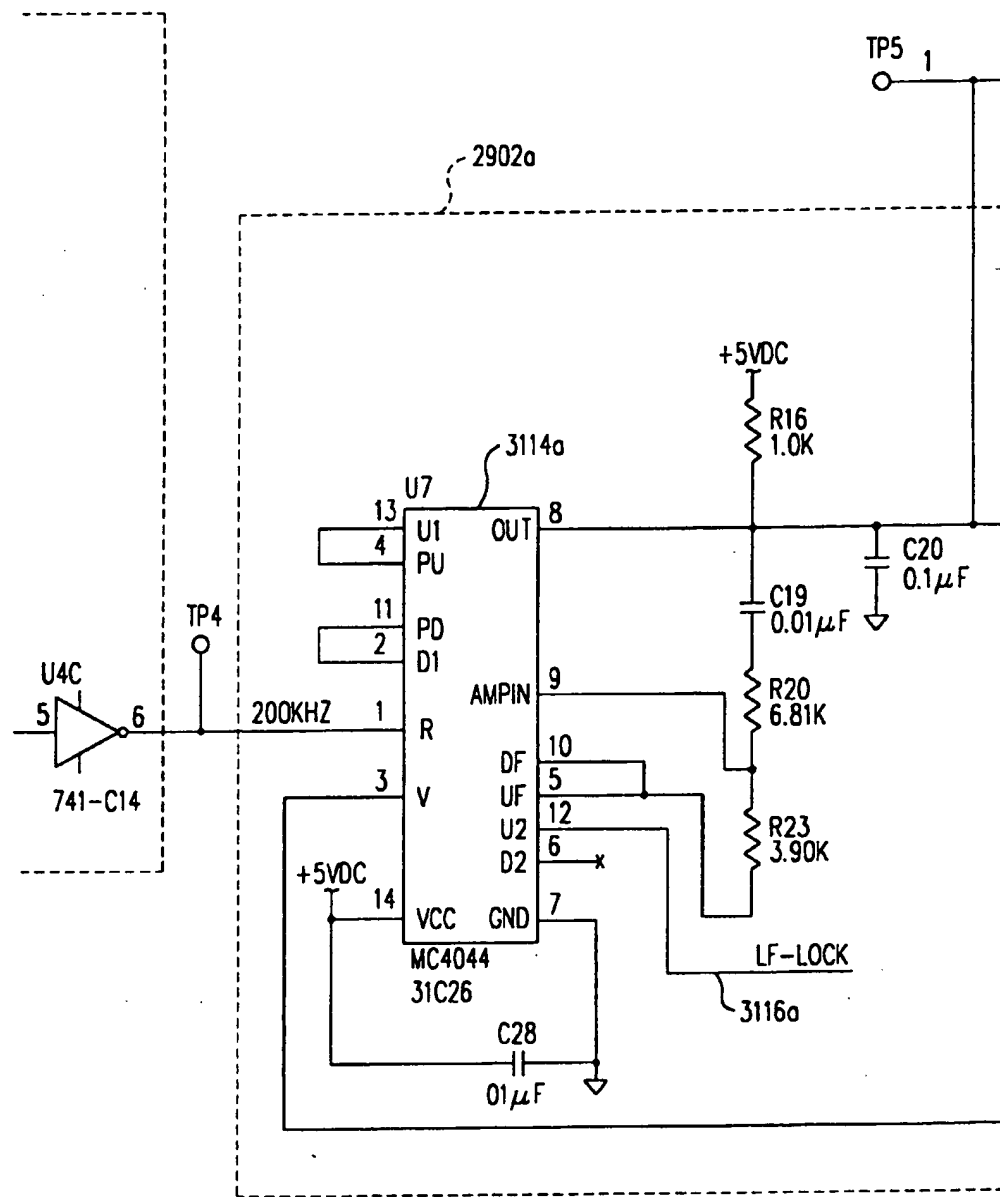


Fig. 31B

LF-E

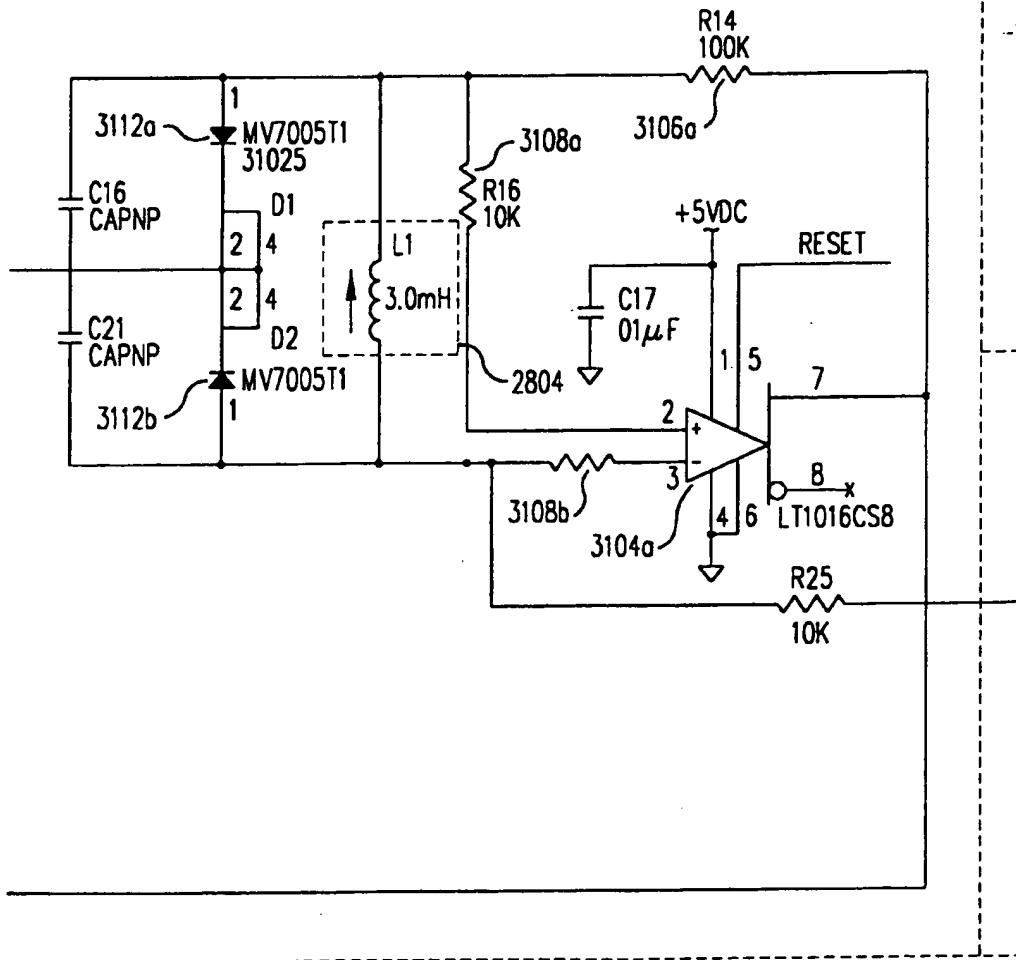


Fig. 31C

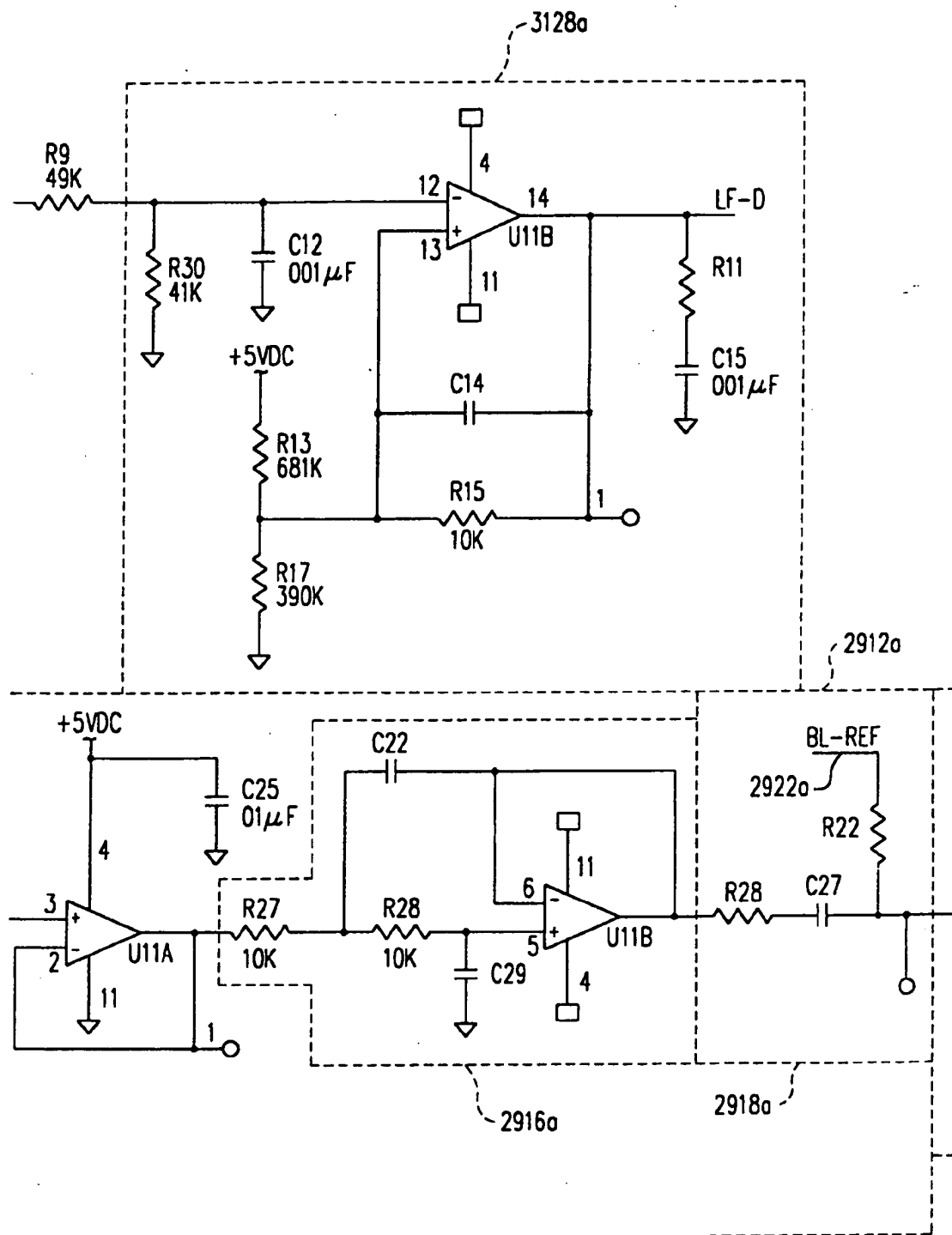


Fig. 31D

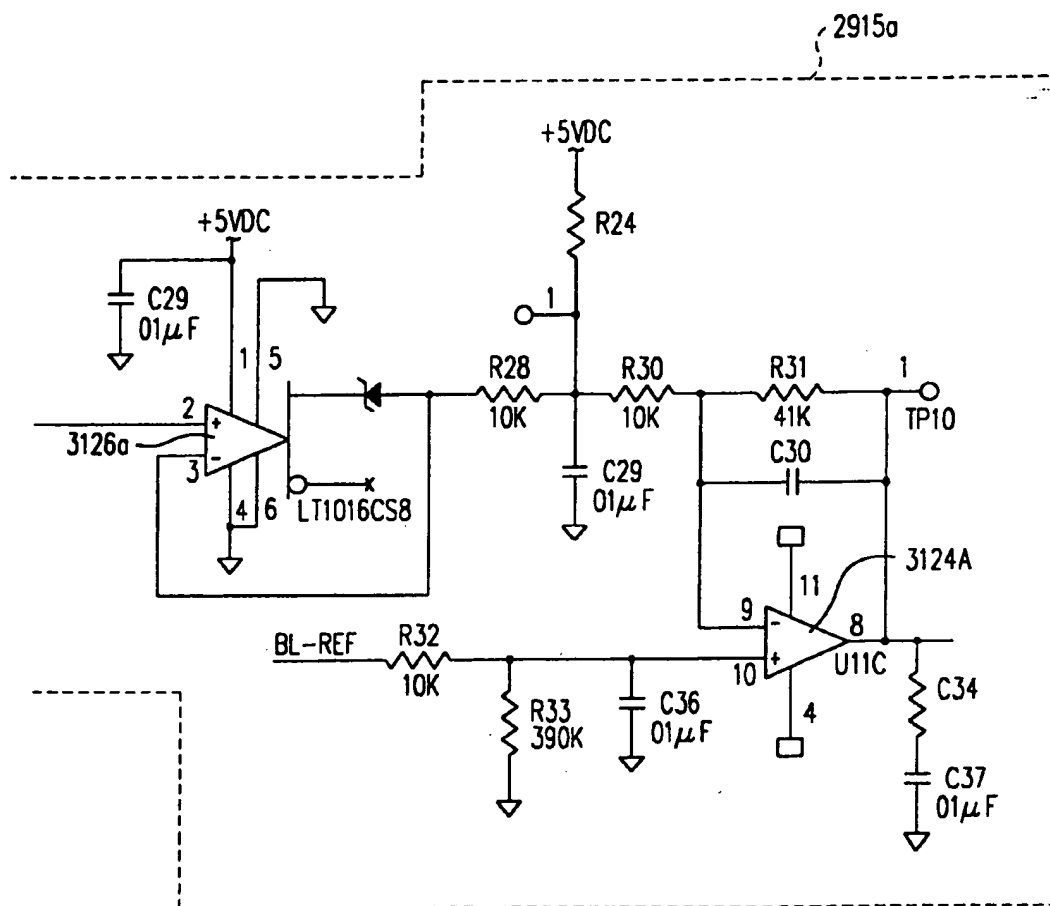


Fig. 31E

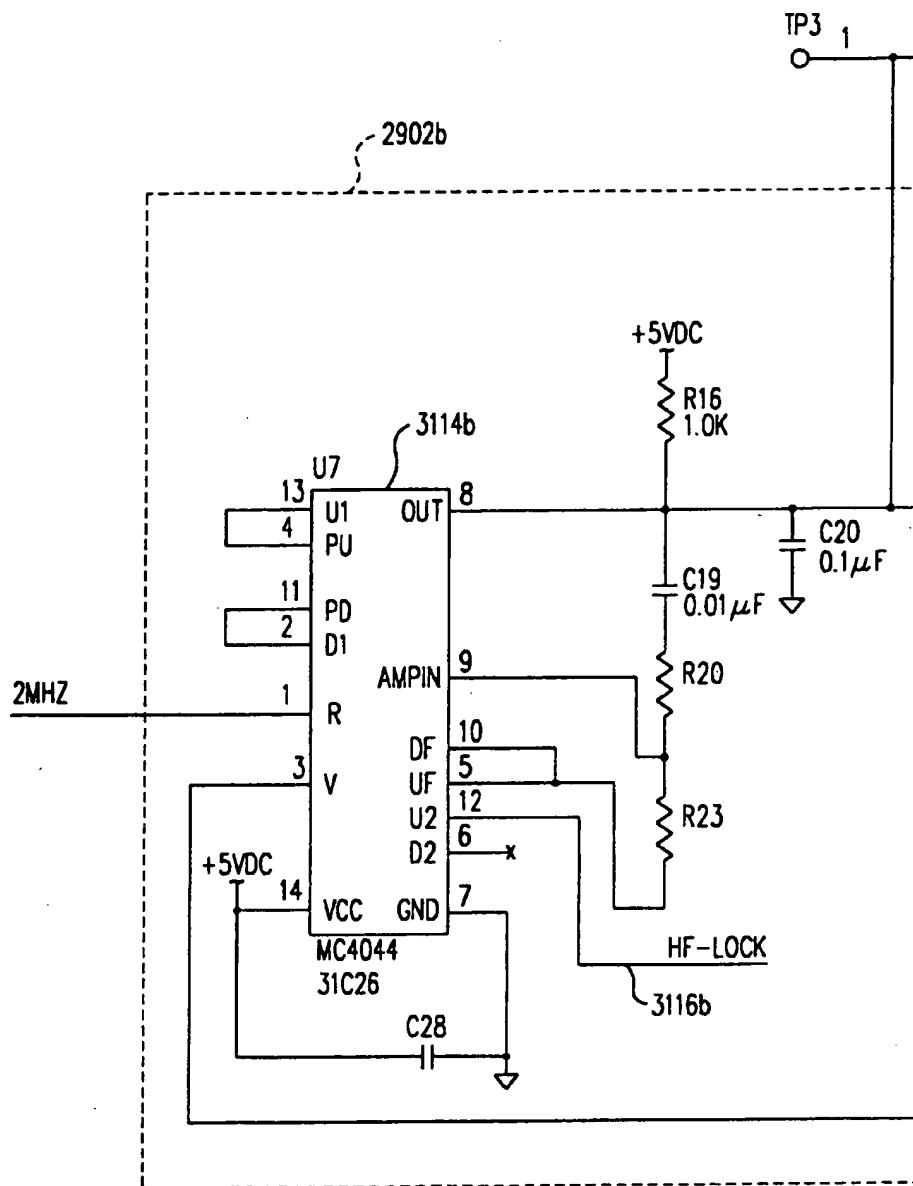


Fig. 31F

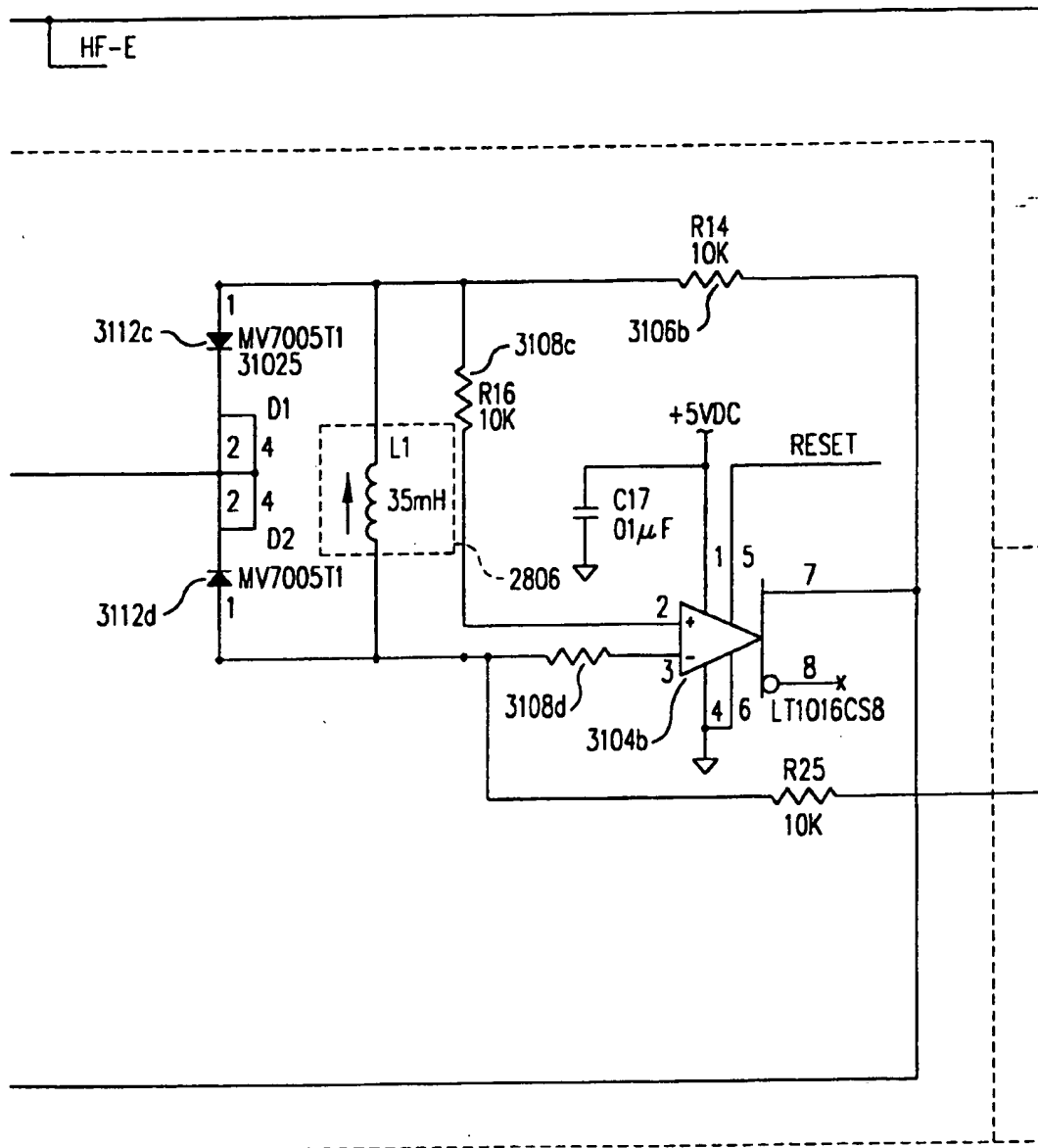


Fig. 31G

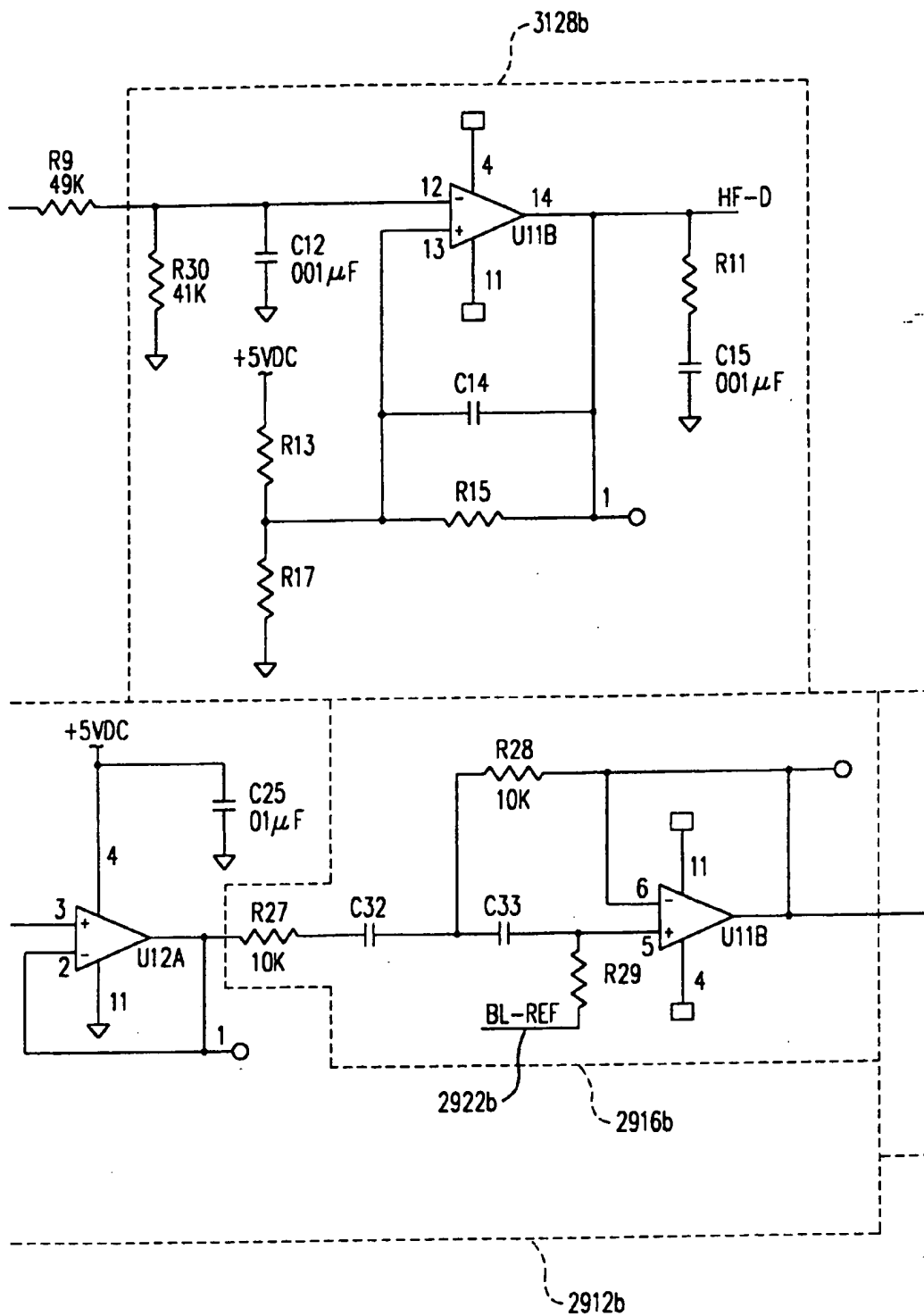


Fig. 31H

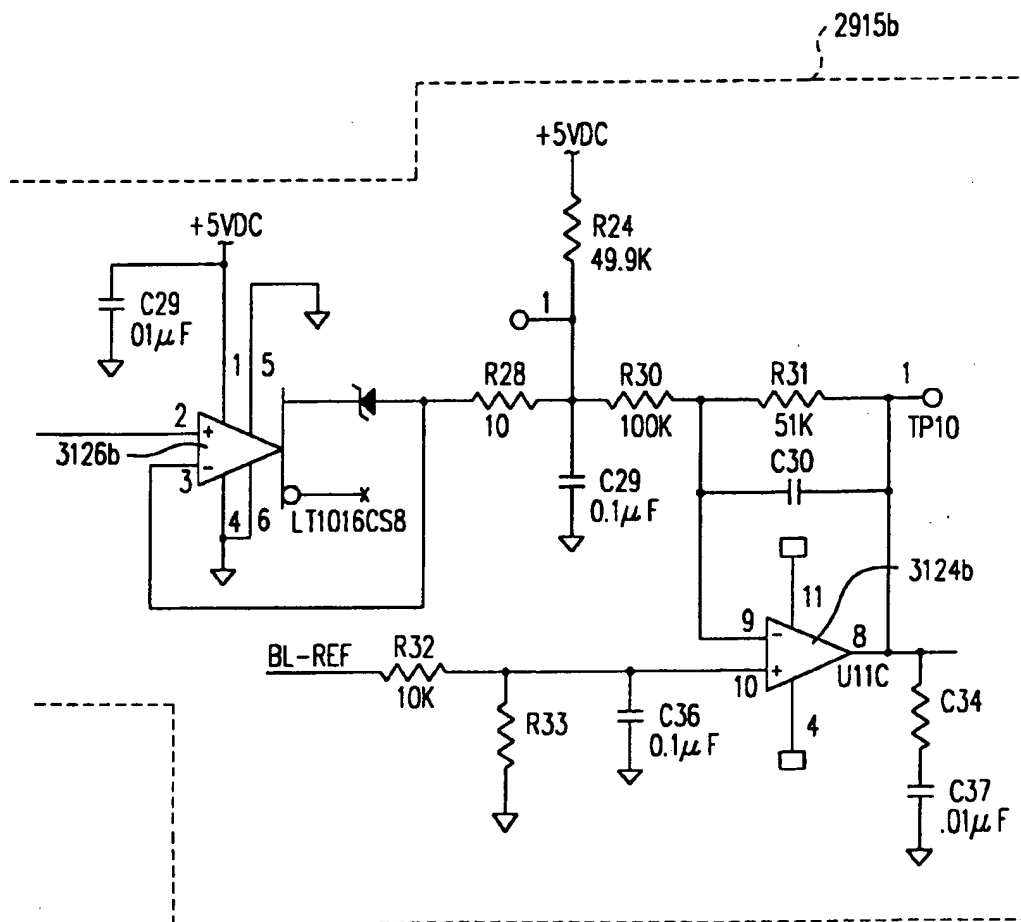


Fig. 31I

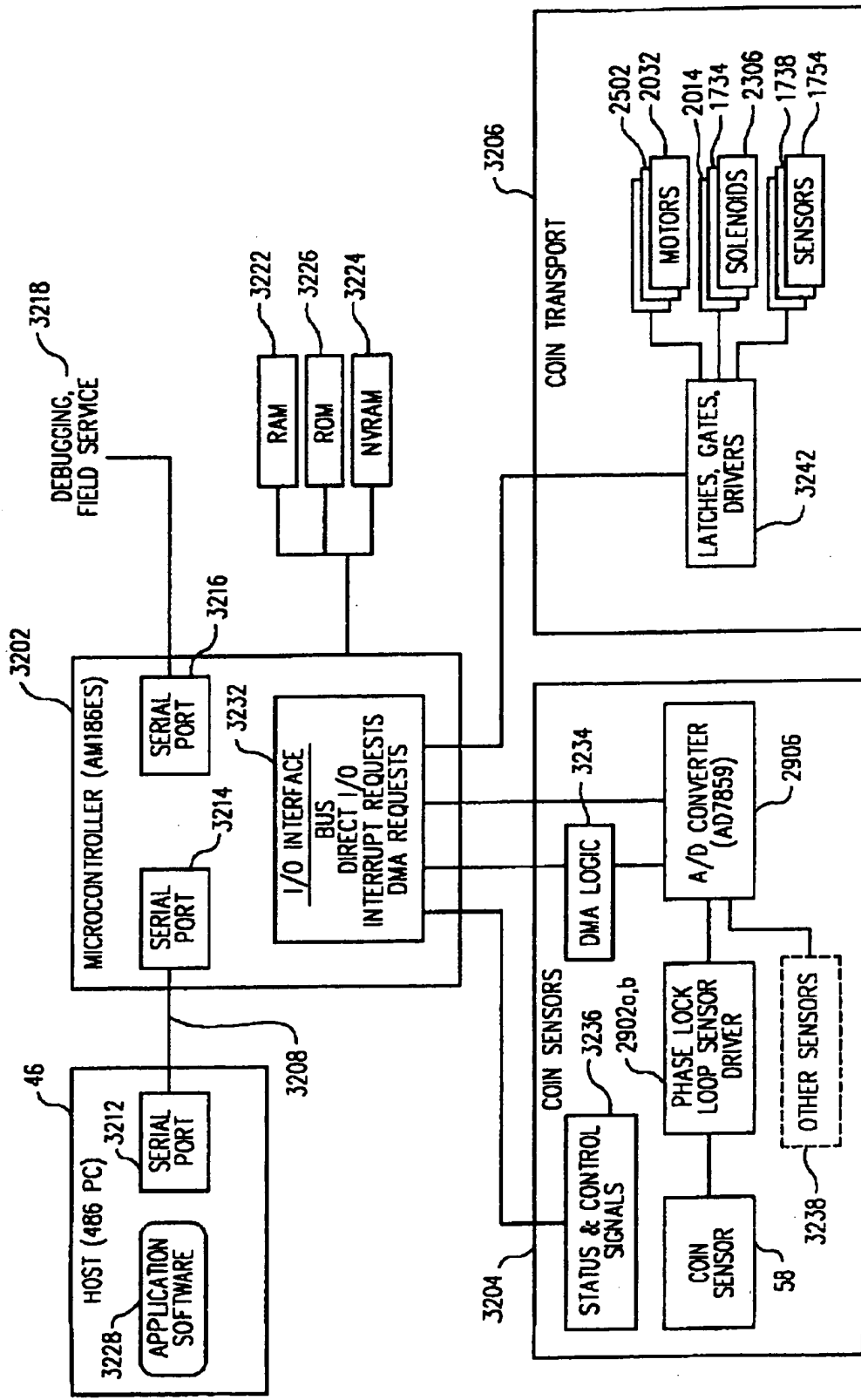


Fig. 32

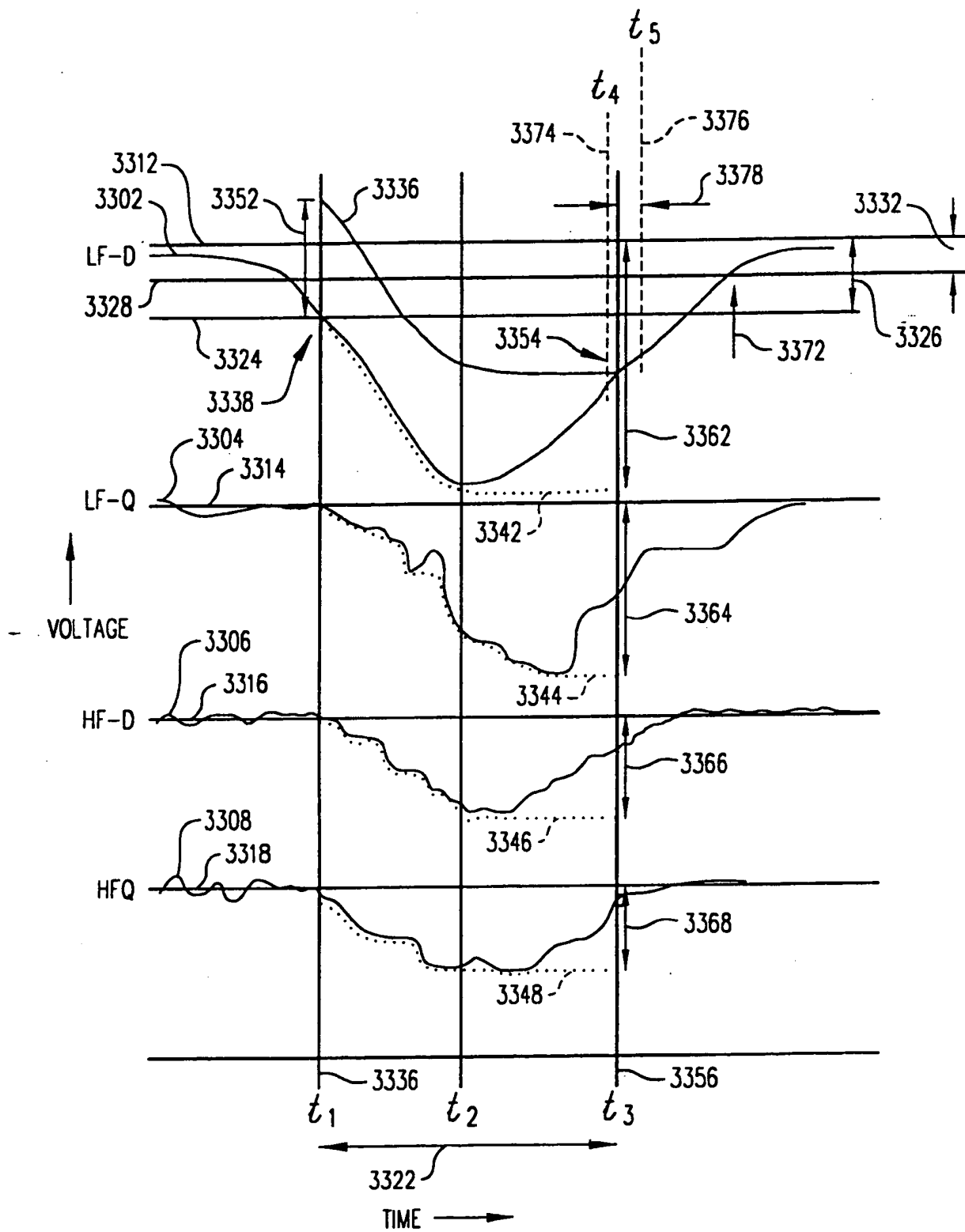


Fig. 33

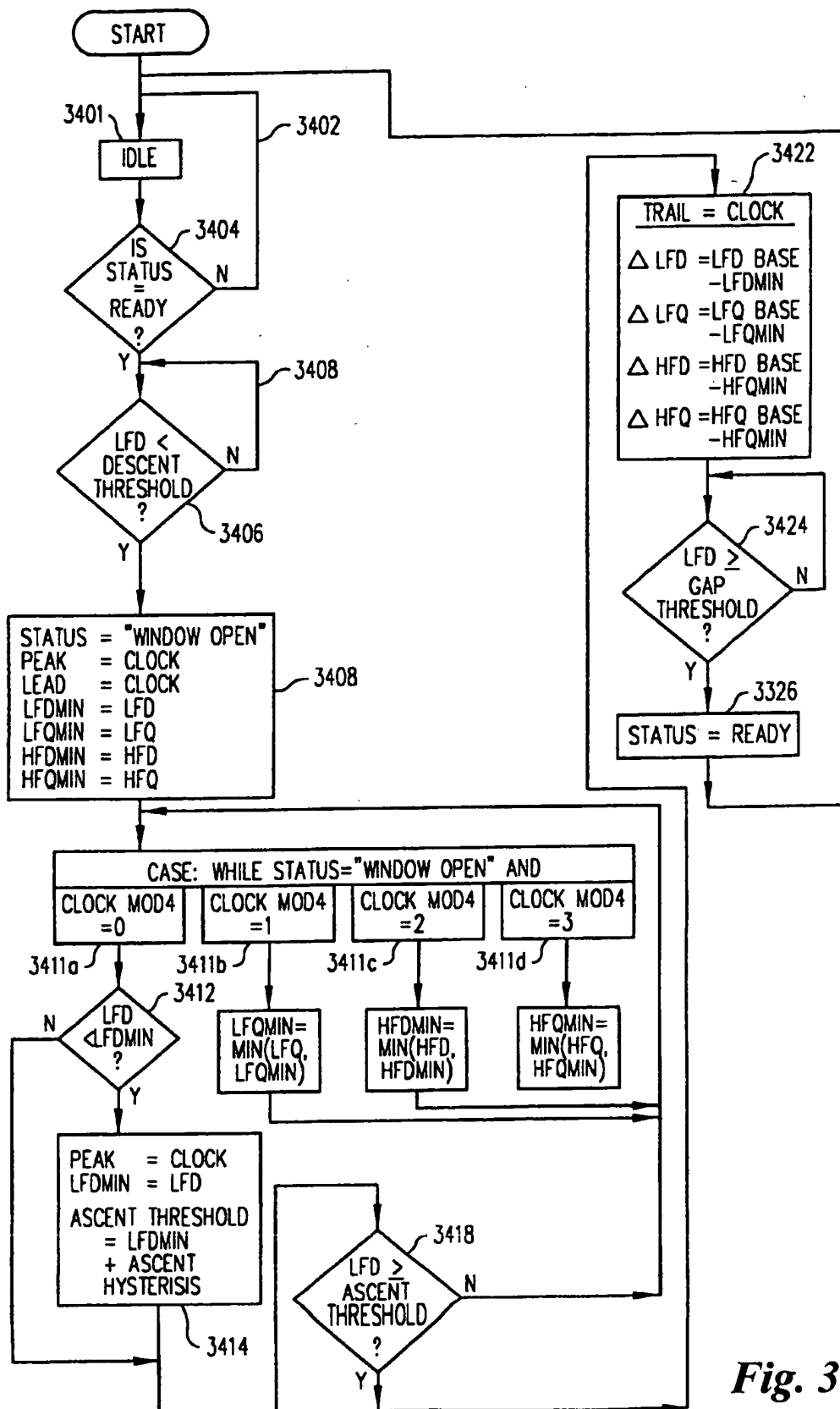


Fig. 34

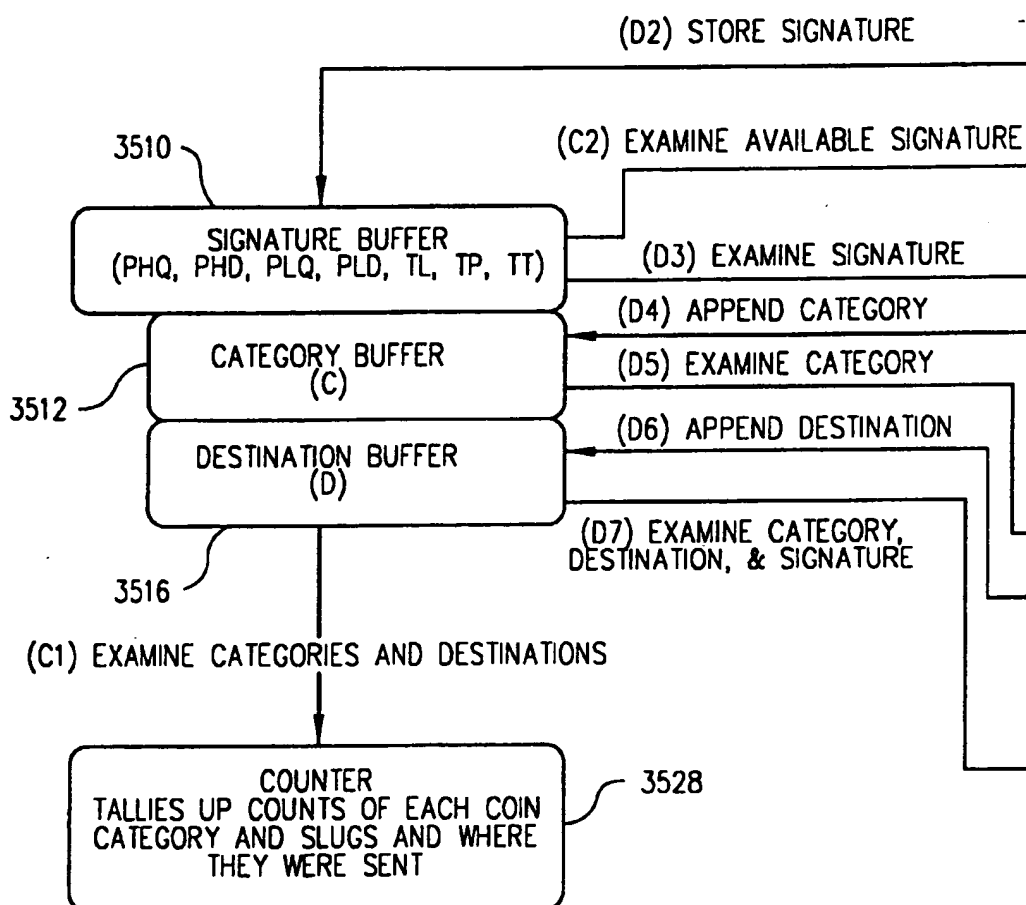


Fig. 35A

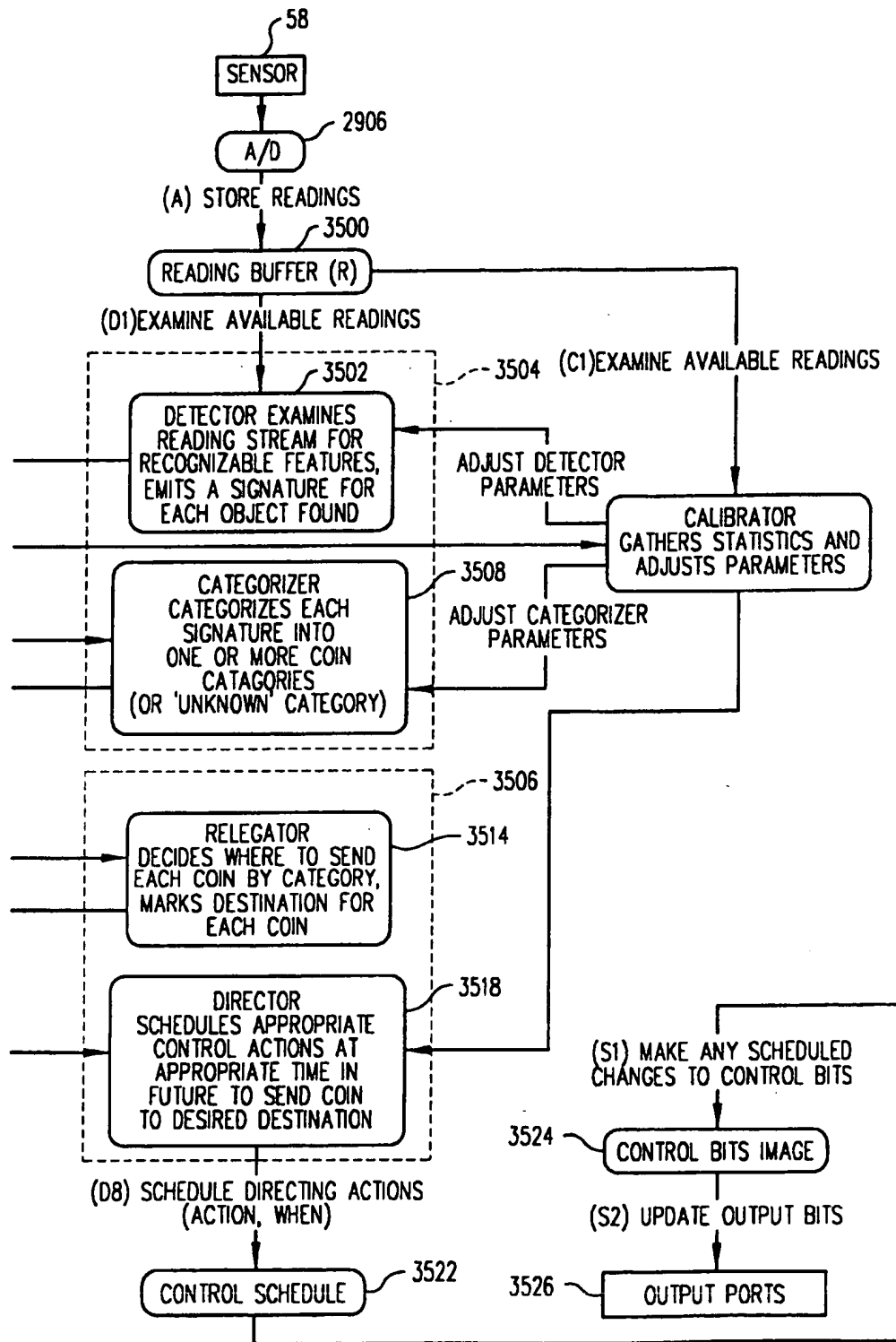


Fig. 35B

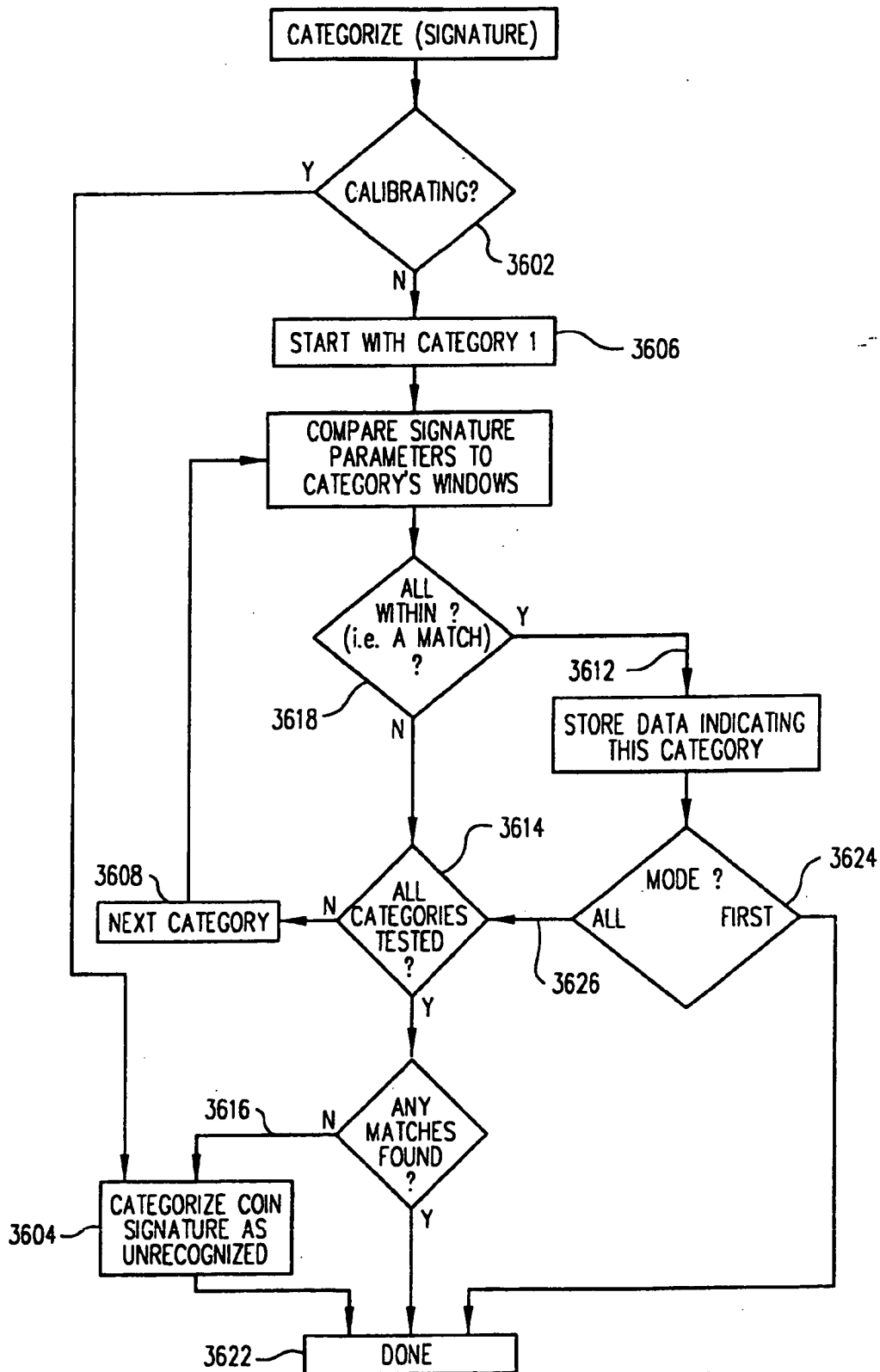


Fig. 36

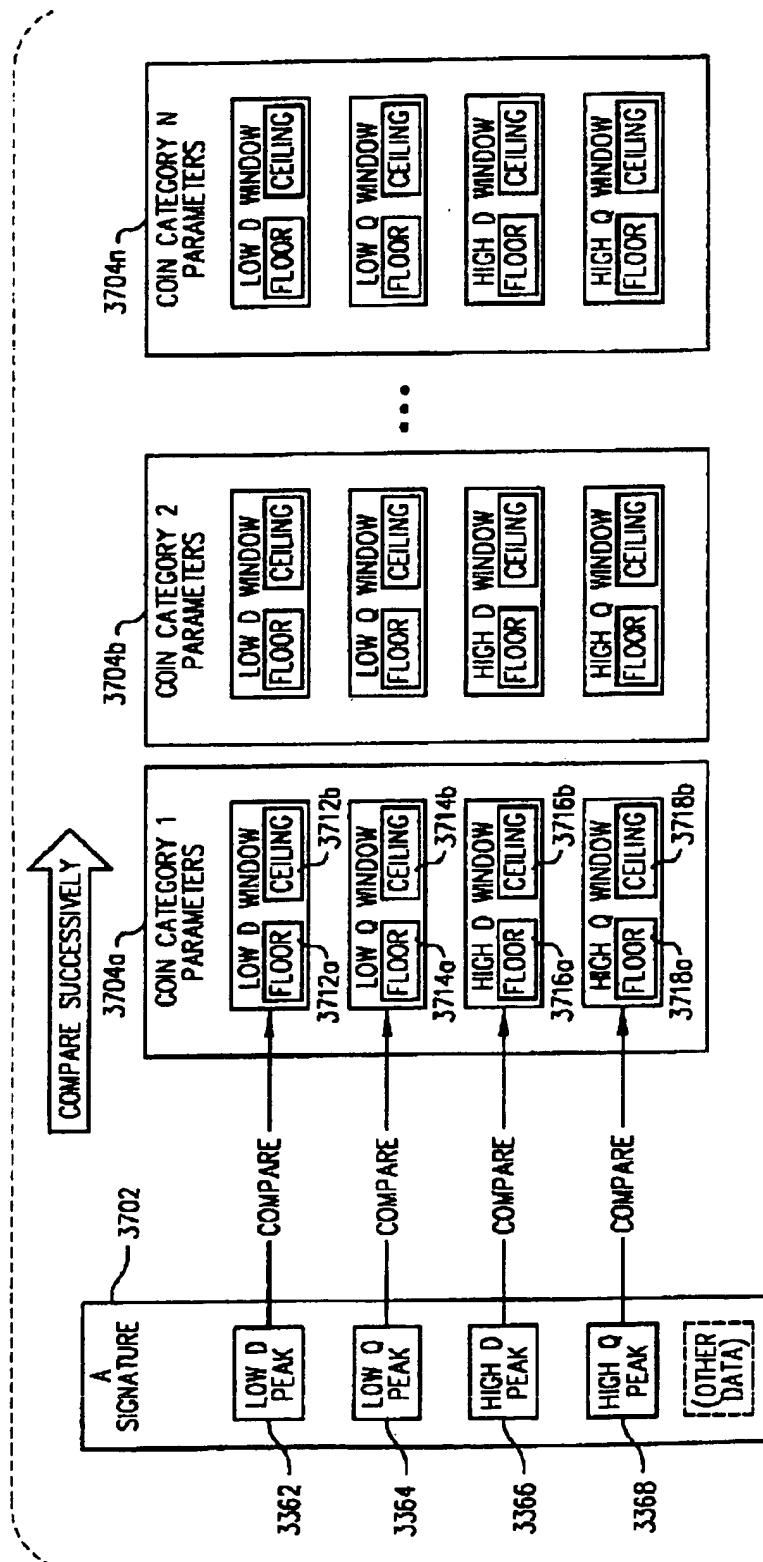


Fig. 37

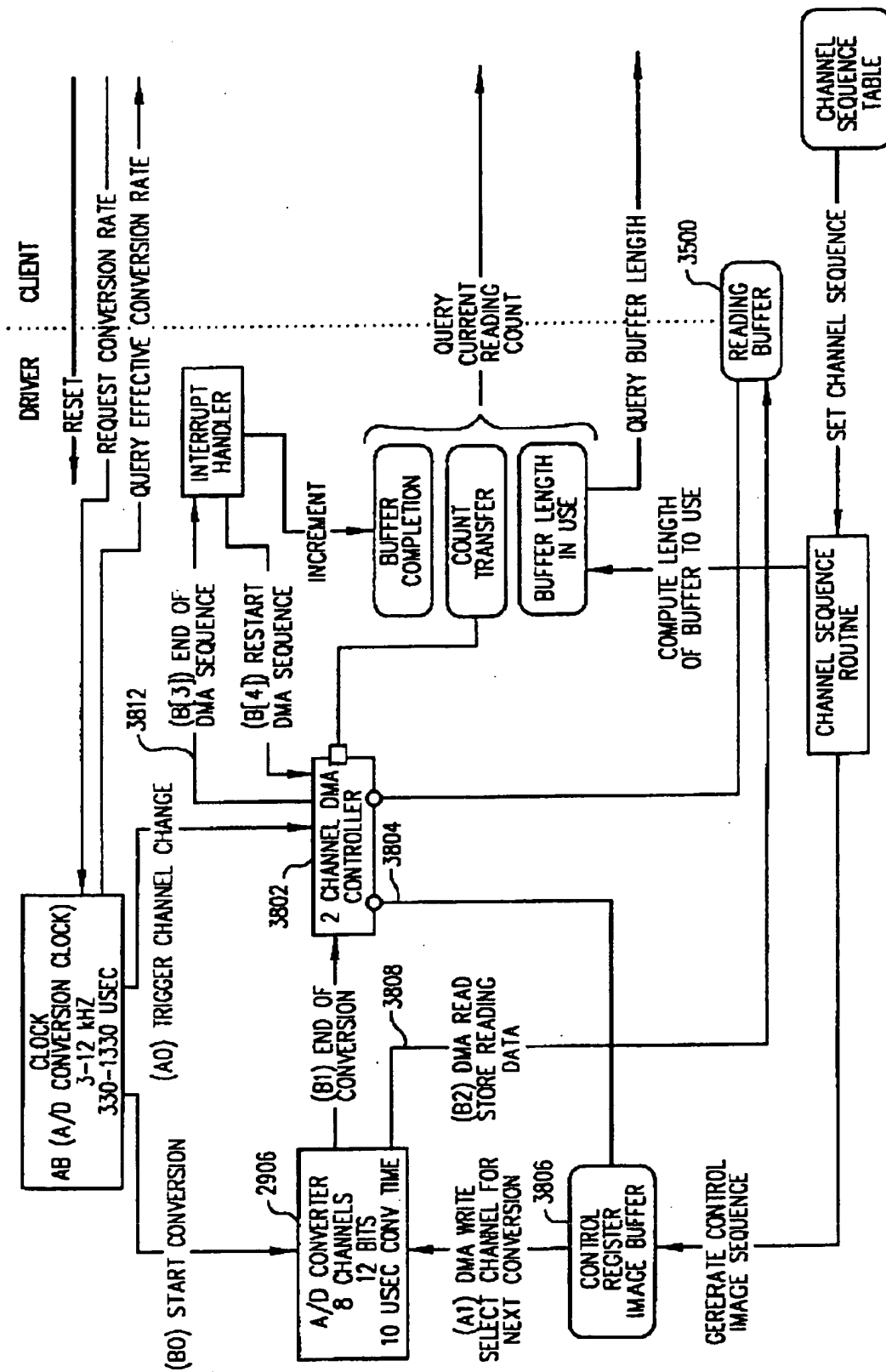
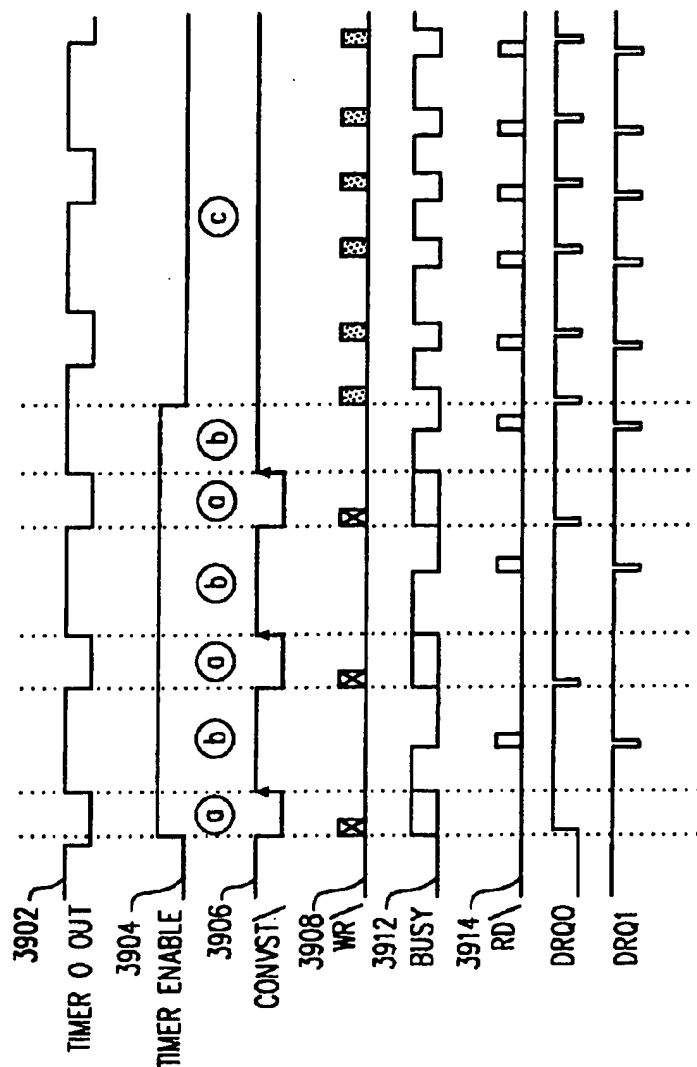


Fig. 38



- (a) DMA1 NOT ALLOWED TO READ DMA0 WRITE EVENT WITH CONVST BIT NOT SET
- (b) DMA0 NOT ALLOWED TO WRITE DMA0 WRITE EVENT WITH CONVST BIT SET
- (c) DMA0 & DMA1 NOT RESTRICTED BY TIMER OUTPUT DMA1 READ EVENT

Fig. 39

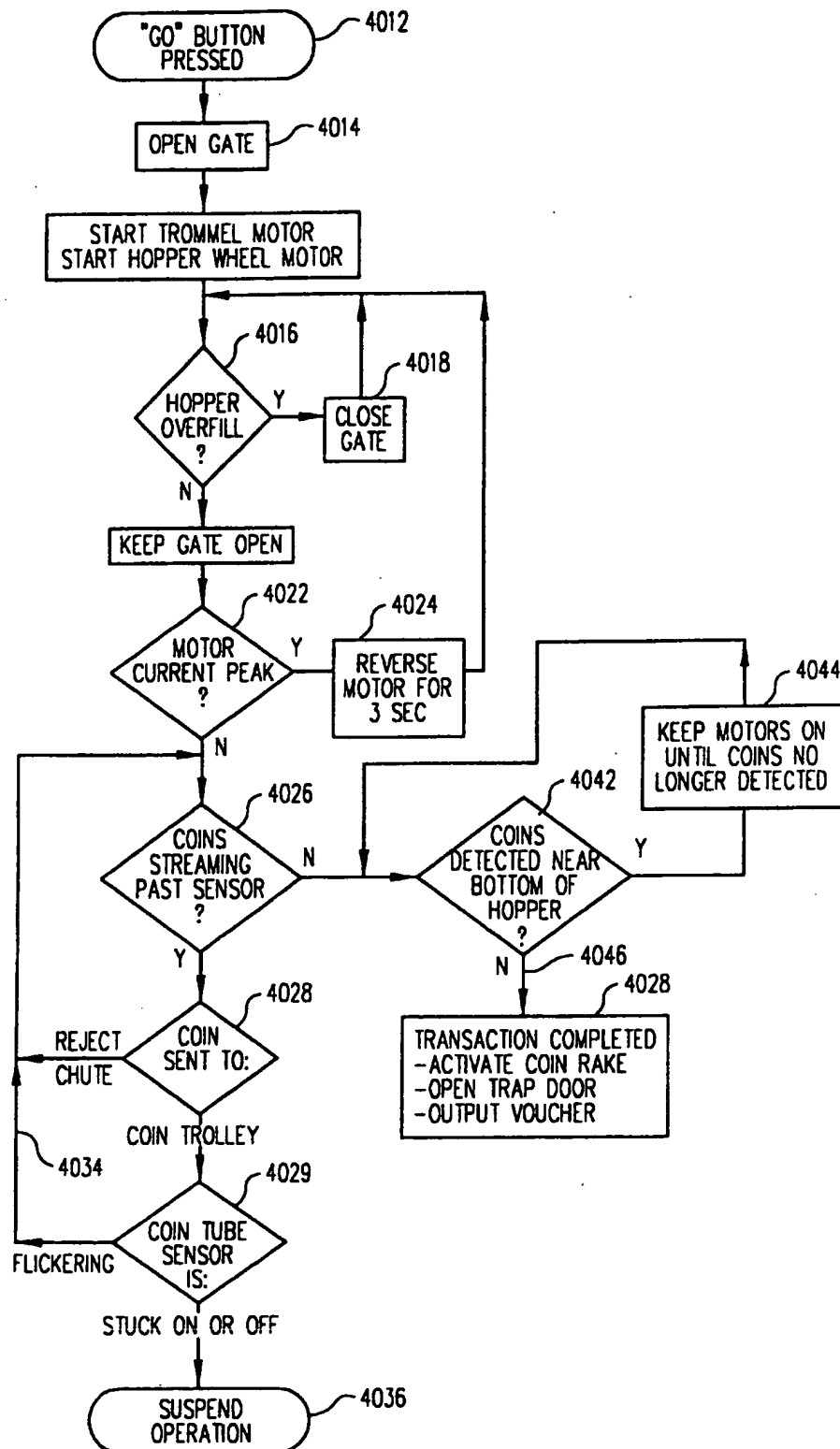


Fig. 40

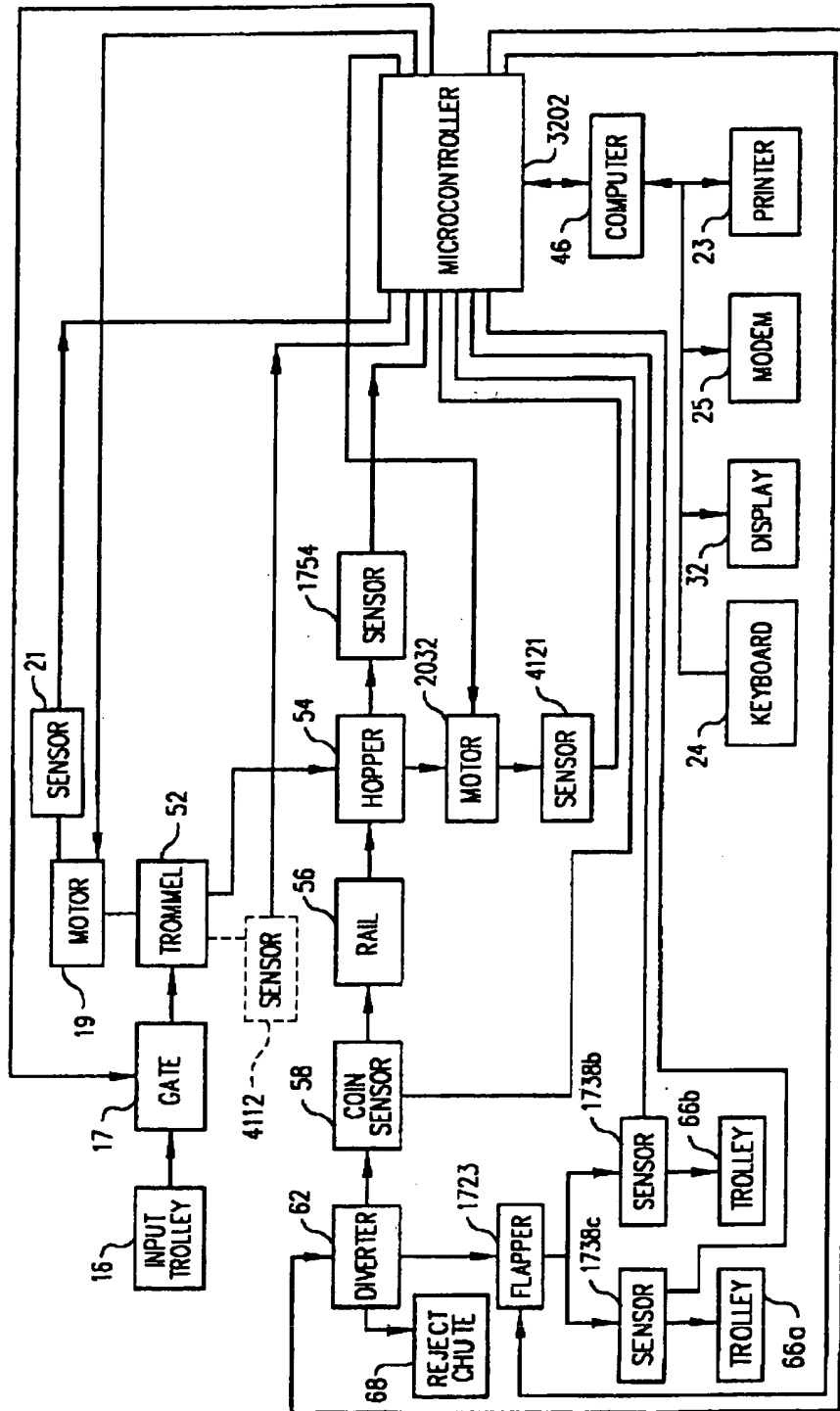


Fig. 41

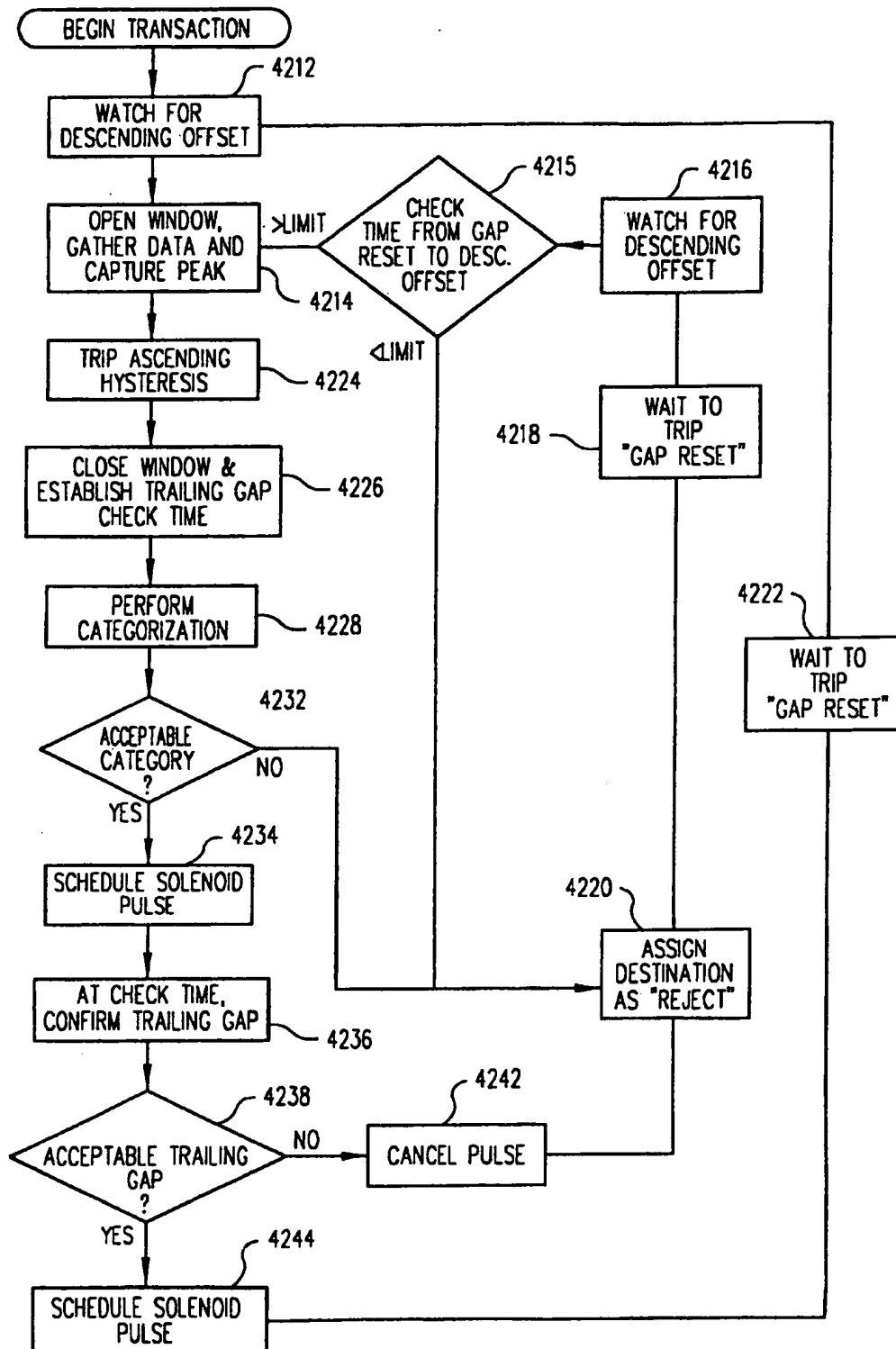


Fig. 42

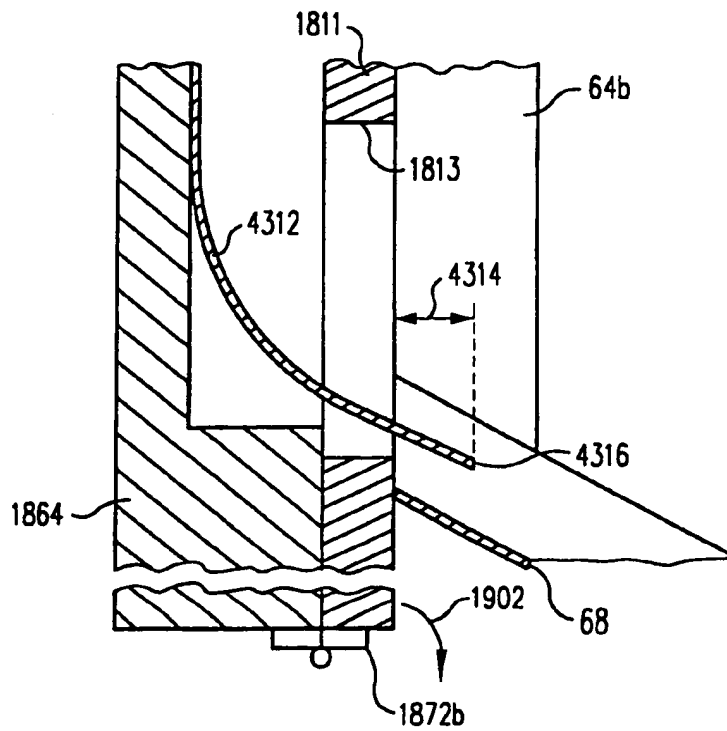


Fig. 43

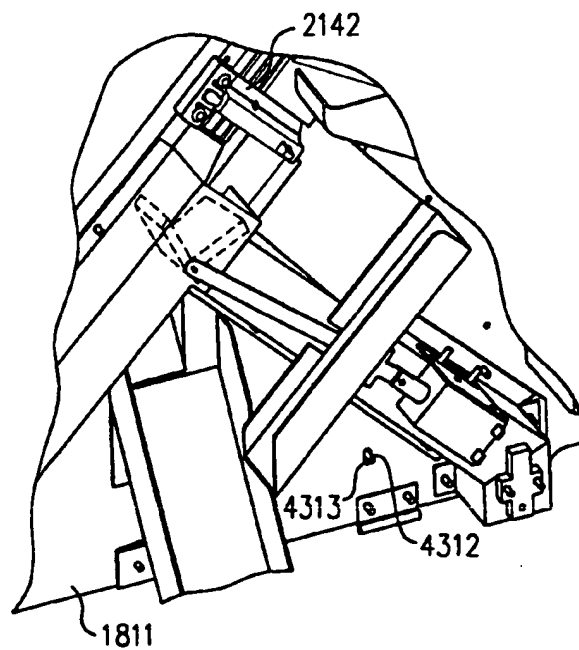


Fig. 43A

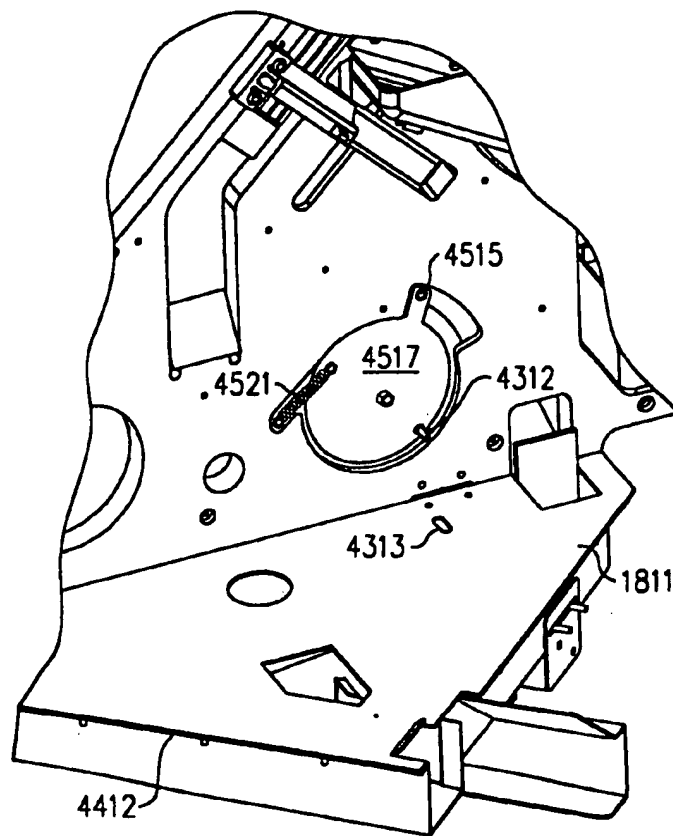


Fig. 44

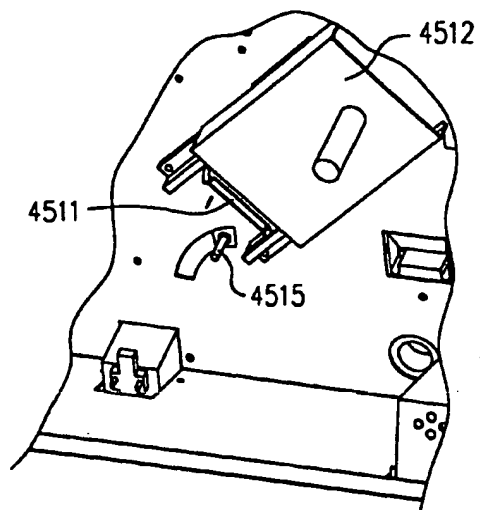


Fig. 45

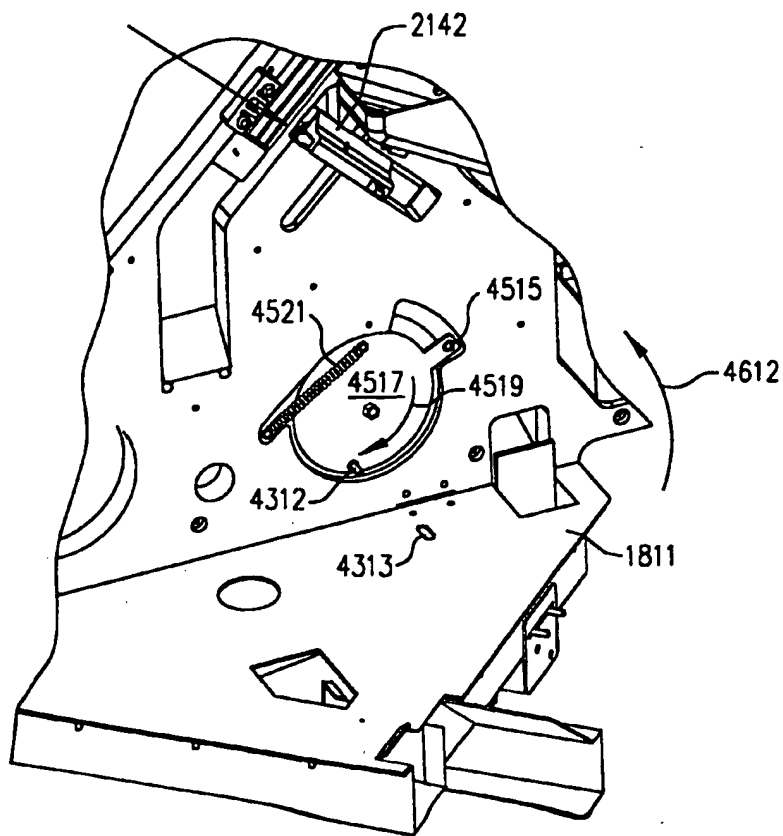


Fig. 46

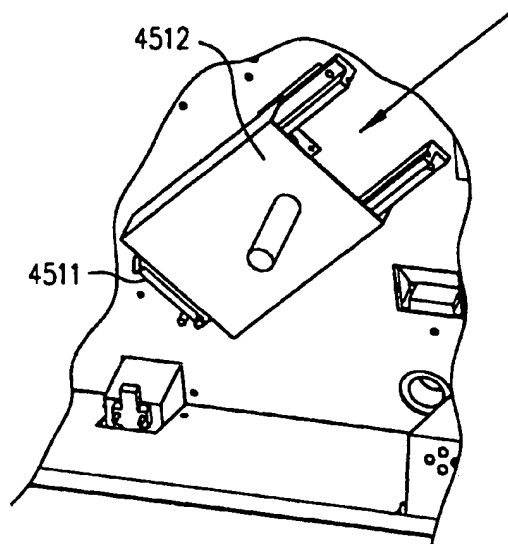


Fig. 47

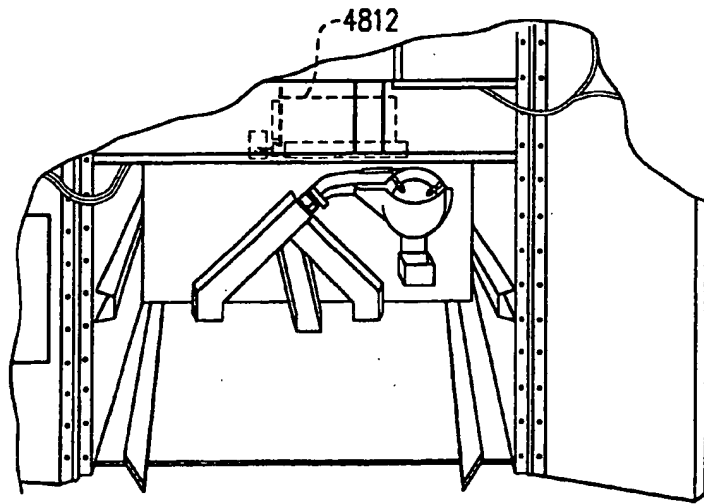


Fig. 48

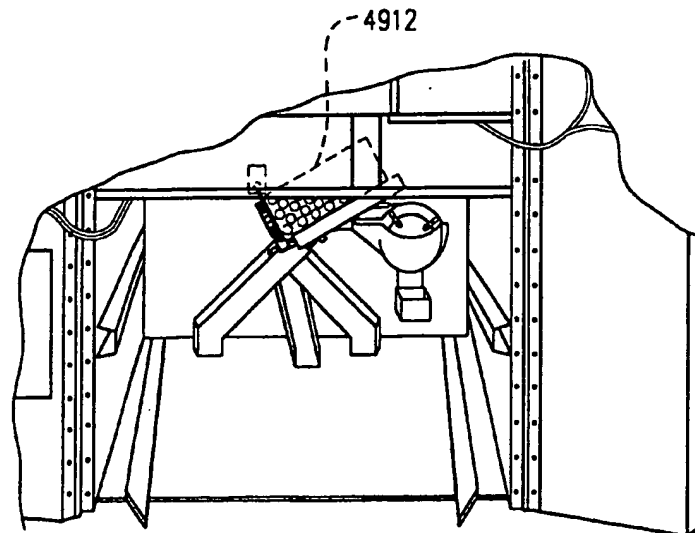


Fig. 49

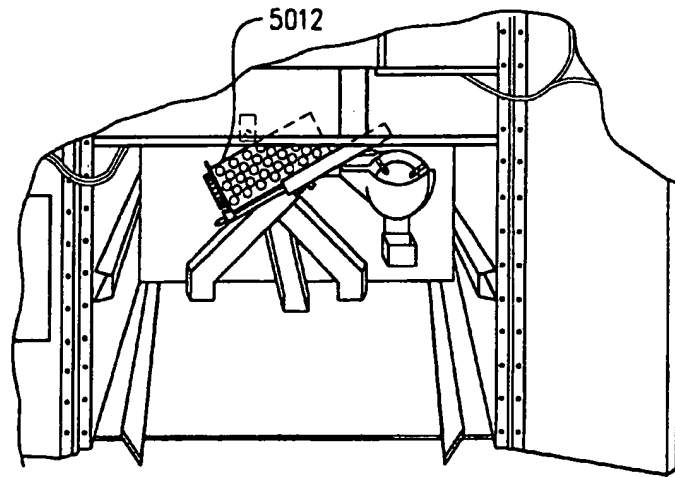


Fig. 50

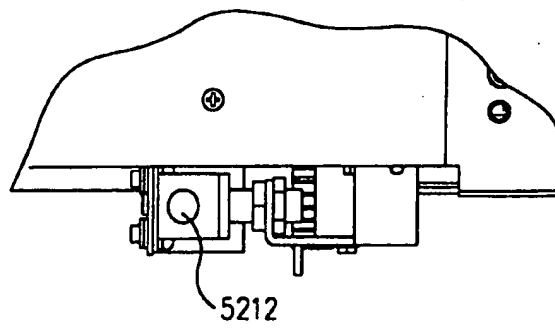


Fig. 52

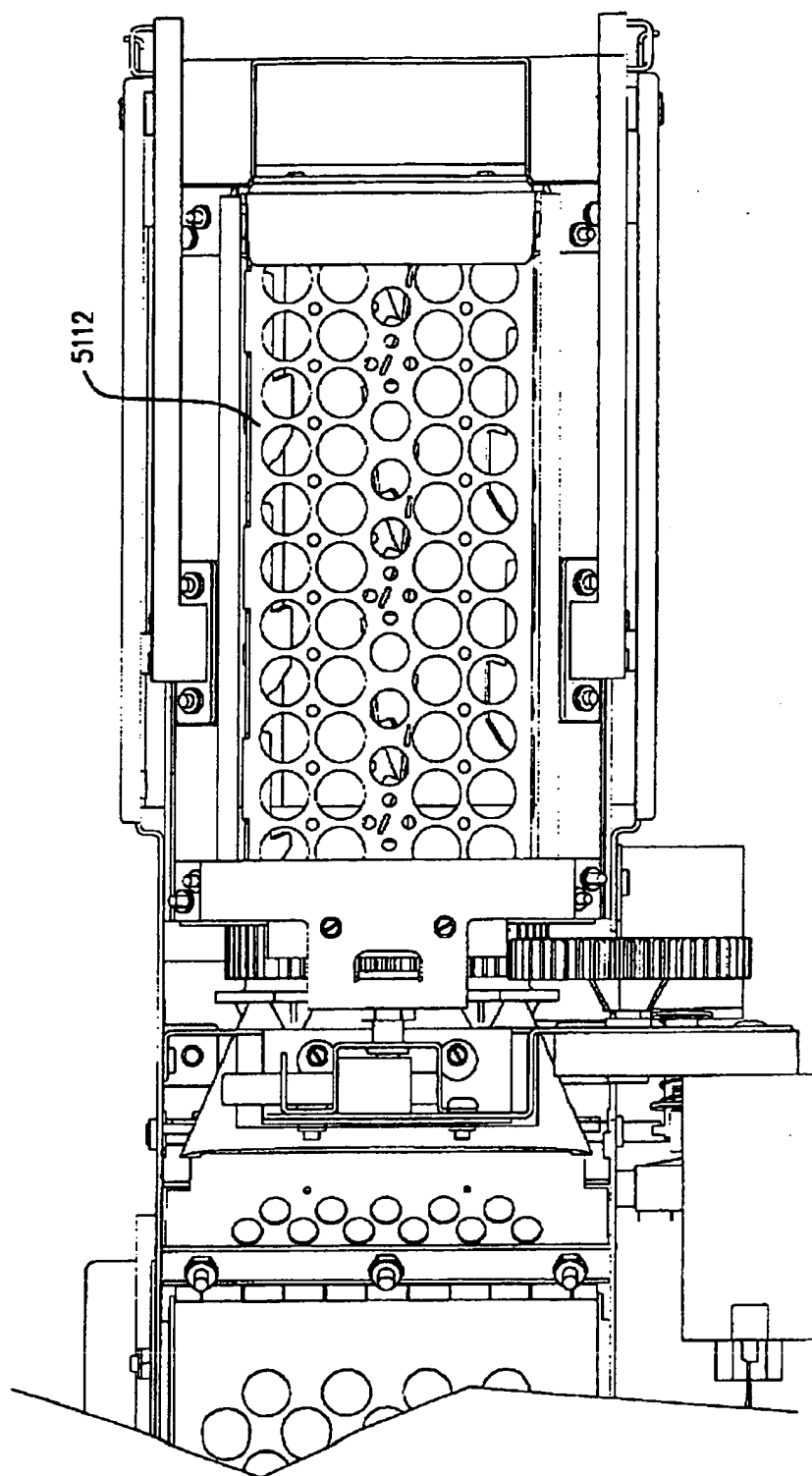


Fig. 51

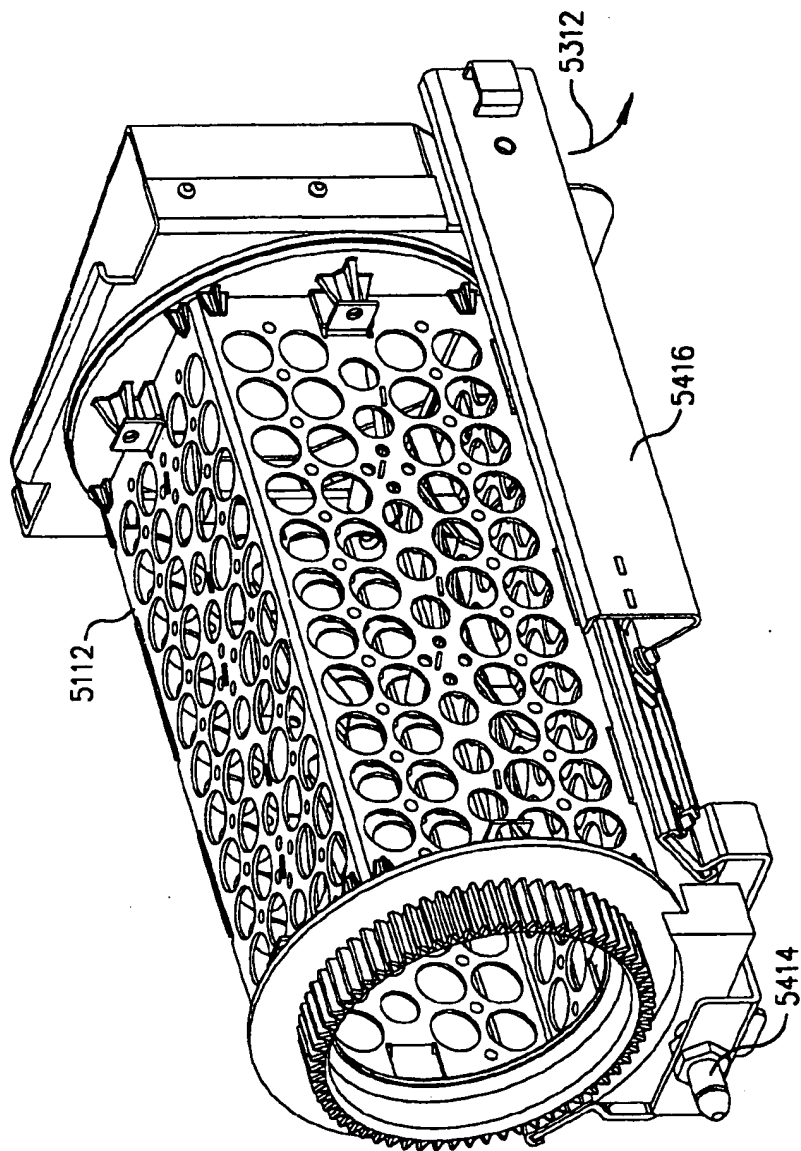


Fig. 53

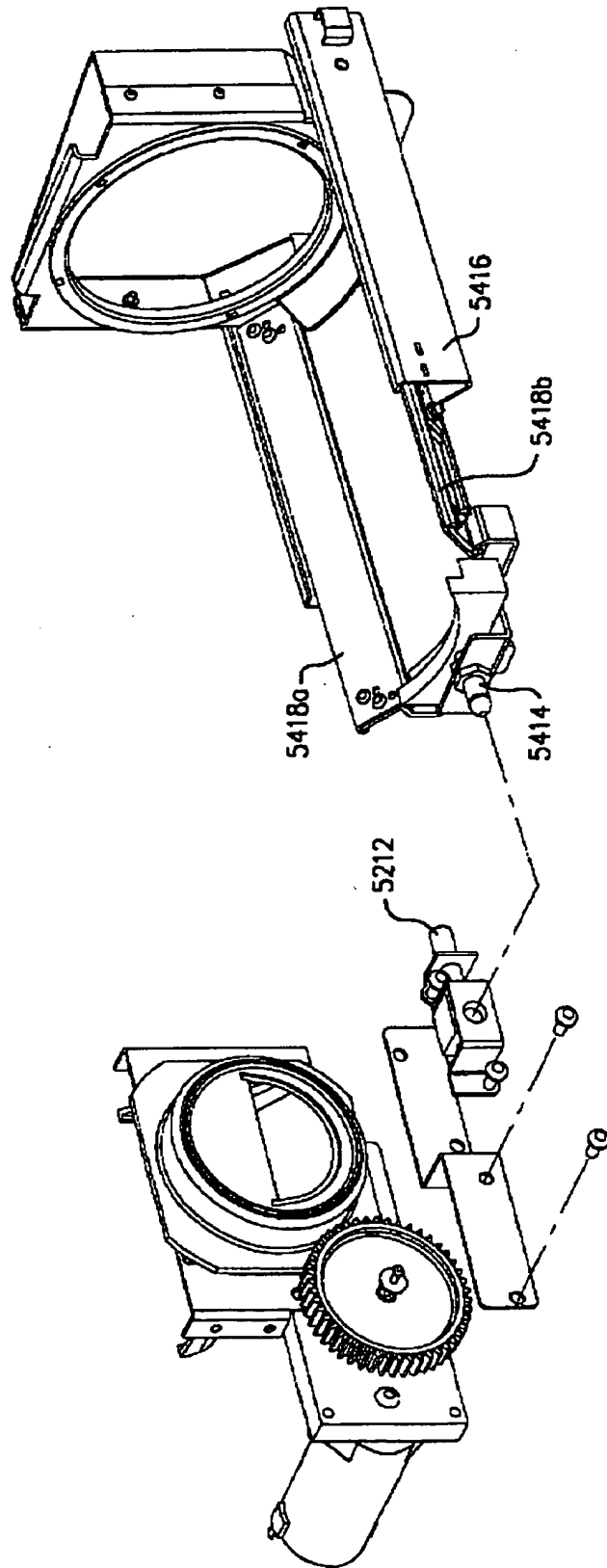


Fig. 54

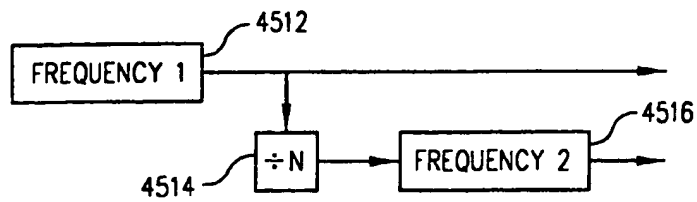


Fig. 55A

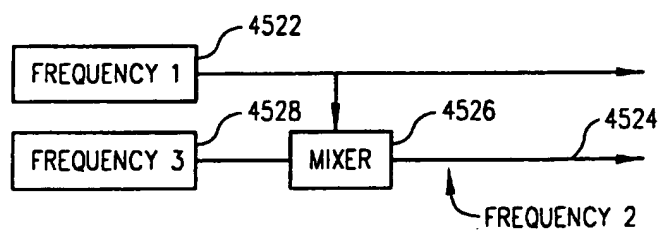


Fig. 55B

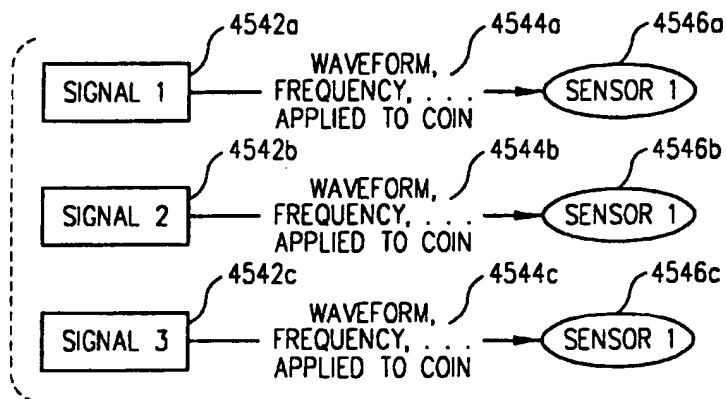


Fig. 55C

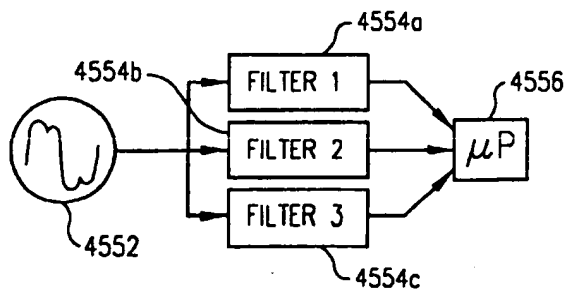


Fig. 55D

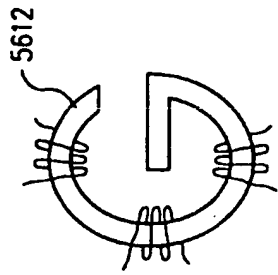


Fig. 56A

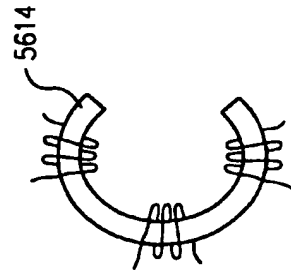


Fig. 56B

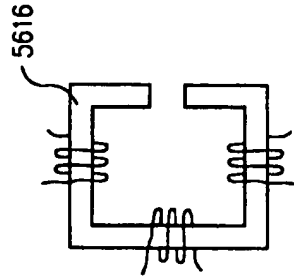


Fig. 56C

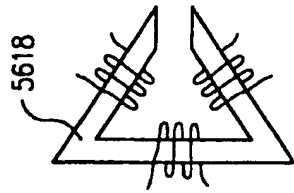


Fig. 56D

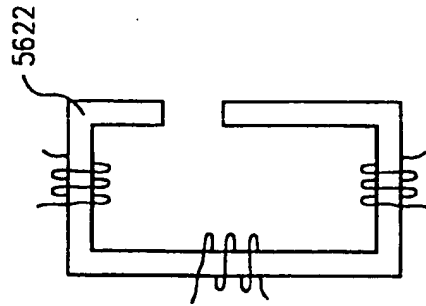


Fig. 56E

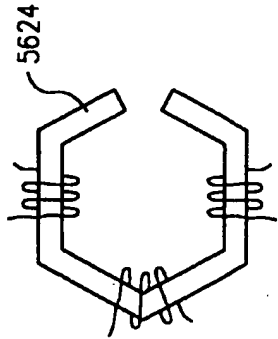


Fig. 56F

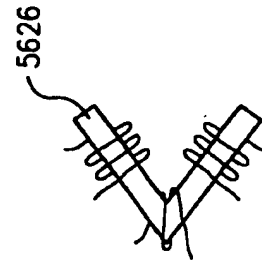


Fig. 56G

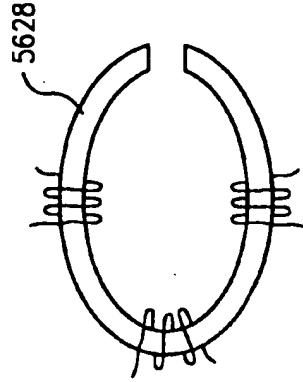


Fig. 56H